EXPERIMENTAL STUDIES ON MULTI-OPERAND ADDERS

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Abstract- ***In this paper, different multi-operand adders have been analyzed in terms of propagation delay, power consumption and resource utilization. The functionality of the adders have been verified using Verilog hardware description language and synthesized in Xilinx ISE. The device chosen for implementation is Virtex 6 (XC6VLX240T) with FF1156 package. Simulation results show that Wallace tree adder is the fastest adder and consumes least amount of power. The Wallace tree adder also consumes the least amount of hardware resources as per the synthesis results.***

Index terms: Multi-operand adders; synthesis results; tree adders; Verilog.