HARDWARE IMPLEMENTATION OF METHODOLOGIES OF FIXED POINT DIVISION ALGORITHMS

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Abstract- This paper describes the hardware implementation methodologies of fixed point binary division algorithms. The implementations have been extended for the execution of the reciprocal of the binary numbers. Radix-2 (binary) implementations of digit recurrence and multiplicative based methods have been considered for comparison. Functionality of the algorithms have been verified in Verilog hardware description language (HDL) and synthesized in Xilinx ISE 8.2i targeting the device xc4vlx15-12sf363 of Virtex4 family. Implementation was done for both signed and unsigned number systems, having bit width of operands vary as an exponential function of 2^n***, where*** n***=2 to 5. Performance parameters have been calculated in terms of clock frequency, FPGA slice utilization, latency and power consumption. Implementation results indicate that multiplicative based algorithm is superior in terms of latency, while digit recurrence algorithms are consuming low power along-with less area overhead.***

Index terms*: Digit recurrence, Division algorithm, Fixed point, FPGA, Newton-Raphson, Verilog.*