DESIGN OF SRAM ARCHITECTURE WITH LOW POWER WITHOUT AFFECTING SPEED USING FINFET

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Abstract- In average 8T SRAM Architecture, it requires maximum number of transistor counts and does not need any write back scheme. To achieve the higher word line (WL) Voltage, the bit line (BL) is connected to the gate of the read buffer SRAM Architecture. That boosted voltage is not used when the threshold voltage is high. Its leads to the reduction of read stability of the SRAM Design. In that case, the gate terminal of the SRAM Architecture is not connected to the buffer results a large delay. To overcome the disadvantage of the average 8T SRAM architecture, the 6T SRAM Design is proposed. In proposed 6T SRAM Design, the number of transistor counts and Power is reduced than the existing design. Various factors of the proposed SRAM Architecture, which stores multiple bits in terms of power and transistor counts. The simulation of 6T SRAM design is carried out in S-Edit and the synthesized in T-Spice.

Index terms: Static random access memory (SRAM), Low voltage operation, Low power consumption,