DESIGN OF LOW LEAKAGE CURRENT AVERAGE POWER CMOS CURRENT COMPARATOR USING SVL TECHNIQUE WITH PSEUDO NMOS AND TRANSMISSION GATE LOGICS

[1]T.R.Dinesh Kumar ,[2]K.Mohana Sundaram[1] M.Anto Bennet[1]*[3]M.Pooja ,[3] A.P. Kokila

[3]K.Anusuya

[1]Faculty of Electronics and Communication Engineering,Vel Tech,Chennai,Tamilnadu,India

[2]Faculty of Electrical and Electronics Engineering,Vel Tech Multitech Dr. Rangarajan Dr. Sakunthala Engineering College,,Chennai,Tamilnadu,India

[3]UG Student of Electronics and Communication Engineering,Vel Tech,Chennai,Tamilnadu,India

* Email: bennetmab@gmail.com

Submitted: May 27, 2017 ***Accepted: June 15, 2017*** ***Published: Sep 1, 2017***

Abstract- Comparatorare most widely used second electronic components after operational amplifier. For ADC circuit we have to use the high speed and low power consumption based comparator. SVL circuit is used tom reduce the offset voltage which requires high voltage gain. A SVL circuit can supply maximum DC voltage to an active load circuit on request or can decrease the DC voltage supplied to a load circuit in the standby mode was developed. SVL circuit is used with comparator which reduce the power consumption from 258.6µw to 156.7µw. Pseudo nmos logic and transmission gate logic is used with the SVL based current comparator which further reduce the power consumption in the standby mode. This technique based comparator is fabricated on the tanner tool of 45nm technology.SVL technique is mostly recommended for CMOS logic.

Index terms: current comparator, SVL circuit, pseudo nmos, transmission gate, low power consumption, standby mode.