EFFICIENT APPROACHES FOR DESIGNING THE LOGICAL REVERSIBILITY OF COMPUTATION

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Submitted: May 27, 2017 ***Accepted: June 15, 2017*** ***Published: Sep 1, 2017***

Abstract-The work demonstrates about the reversible logic synthesis for the 2 to 4 decoder, the circuits are designed using reversible fault tolerant toffoli gates. Thus the entire scheme inherently becomes fault tolerant. In addition, several lower bounds on the number of constant inputs, garbage outputs and quantum cost of the reversible fault tolerant decoder have been proposed. Transistor simulations of the proposed decoder power consumption have been reduced than the existing approach without decreasing the speed, which proved the functional correctness of the proposed Decoder. The comparative results show that the proposed design is much better in terms of quantum cost, delay, hardware complexity and has significantly better scalability. Tanner software is the advanced industrial tool that is growing up in trend. So the proposed decoder is designed in Tanner EDA after completion of the circuit in DSCH and Microwind. This shows the power dissipation and power consumption at each nook and corner to re-design with low power consumption possible.

Index terms*: Fast Fourier Transform (FFT),:Reversible Logic Synthesis(RLS).*