COMPUTATION OF FIELD PROGRAMMABLE CYCLIC REDUNDANCY CHECKS CIRCUIT ARCHITECTURE

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Abstract- In this work we are going to simulate a field programmable cyclic redundancy check circuit architecture. The transmitted data or stored data must be free from error. The increased use of error correction techniques by digital communications designers has created a demand for tools to evaluate and exercise error correction coding approaches before they are committed to expensive ASICs or firmware. Cyclic redundancy check is an error detection method but it can be used only for a specific application. A field programmable circuit is one which enables a wide range of polynomial width and input port width to be used with in the same circuit. The parameters are reprogrammable and it is fully flexible. The circuit also consists of an embedded configuration controller that reduces the programming time and complexity. The hardware cost is reduced and the line speed is increased. The primary tool used is modelsim 6.1a.

Index terms*:* Cyclic Redundancy Check (CRC), Application Specific Integrated Circuit. ASIC.