DESIGN OF LOW LEAKAGE CURRENT AVERAGE POWER CMOS CURRENT COMPARATOR USING SVL TECHNIQUE WITH PSEUDO NMOS AND TRANSMISSION GATE LOGICS

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Abstract- Comparatorare most widely used second electronic components after operational amplifier. For ADC circuit we have to use the high speed and low power consumption based comparator. SVL circuit is used tom reduce the offset voltage which requires high voltage gain. A SVL circuit can supply maximum DC voltage to an active load circuit on request or can decrease the DC voltage supplied to a load circuit in the standby mode was developed. SVL circuit is used with comparator which reduce the power consumption from 258.6µw to 156.7µw. Pseudo nmos logic and transmission gate logic is used with the SVL based current comparator which further reduce the power consumption in the standby mode. This technique based comparator is fabricated on the tanner tool of 45nm technology.SVL technique is mostly recommended for CMOS logic.

Index terms: current comparator, SVL circuit, pseudo nmos, transmission gate, low power consumption, standby mode.

I. INTRODUCTION

Comparators are one of the most important elements for analog circuit design because of low power consumption, minimum size transistors, high speed, small chip area and there are large number of applications such as scientific computation, test circuit application and general purpose processor component. Comparator is very attractive for memory, sensing elements, analog to digital convertors and data receivers. The basic block diagram of comparator is shown in fig.1.1 and fig.1.2.

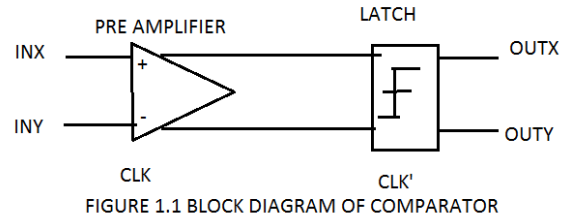

FIGURE 1.1 BLOCK DIAGRAM OF COMPARATOR

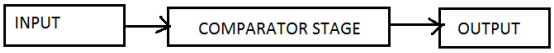

FIGURE 1.2 BLOCK DIAGRAM OF A SIMPLE CURRENT COMPARATOR

II. LITERATURE SURVEY:

There are two well-known existing techniques for reducing stand-by-power(Pst).One is multi threshold voltage cmos(MTCMOS)[10] which reduces Pst by disconnecting the power supply through the P-MOSFET switches(SWs) with higher threshold voltage(Vth).However it has serious drawback that it requires additional fabrication process for higher Vth and storage circuit based on this technique cannot retain data. The another technique is variable threshold voltage cmos(VTMOS) [11] this also faces some problem such as very slow substrate bias controlling operation,large area and power penalty.

To solve this drawbacks, a SVL circuit which decreases the stand by power with high speed performance have been developed. When the loads circuit is in active mode the SVL circuit supplies maximum DC voltages through switches that are turned on i.e., “on SWs” so that it can operate quickly.When the load circuit is in stand by mode it supplies slightly lower Vd and higher Vs through “on SWs” so that Vdsn decreases and Vsub increases. Thus, Vth increases and subthreshold current decreases so that Pst is reduced.

In this paper we have designed the current comparator using SVL technique with pseudo nmos and transmission gate logic style. Thus the result compraising of power

consumption of basic current comparator and SVL based current comparator with these two logics.

III. PROPOSED SYSTEM:

SVL technique which reduces the stand by power with high speed performance was proposed in cmos current comparator with pseudo nmos and transmission gate logic .There are three types of SVL technique type 1 – upper svl, type 2 - lower svl, type 3 – svl circuit (combination of upper and lower svl circuit).

In SVL circuit when control signal (CL) is applied n – sw turns on and p – sw turns off .Vdd is applied to the inverter through n – SWs. Thus, a drain to source voltage (Vdsn) i.e., drain voltage (Vd) of the "off n-mos" can be expressed as

$$Vdsn= Vdd-mv \quad - (1)$$

Where v is the voltage drop of the single n-sw and m is the number of the n-sw used. Vdsn can be changed by varying m or v. Vdsn can be decreased by increasing mv which increases the barrier height of the "off n-mos" which further increase the Vth and reduces the leakage current. The type 1 upper SVL circuit is shown in the figure 3.1.

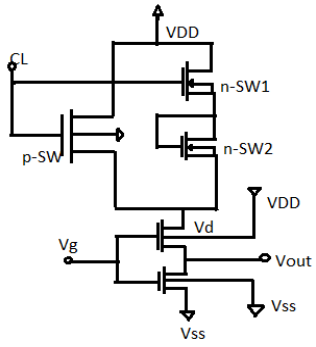

FIGURE 3.1.CIRCUIT OF UPPER SVL

In the lower SVL circuit when negative control signal is applied it turns on p-sw and n-sw is turned off. Vss is supplied through p-SWs. The increase in the gate bias increases the Vth which reduces the threshold current and leakage current. The type 2 lower SVL circuit is shown in the figure 3.2.

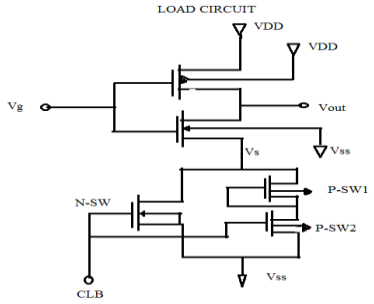

FIGURE 3.2 LOWER SVL CIRCUIT

The working of the type 3-SVL circuit is same as the combination of the upper svl circuit and lower svl circuit and the power consumption is reduced more in this circuit. The type 3 SVL circuit is shown in the figure3.3.

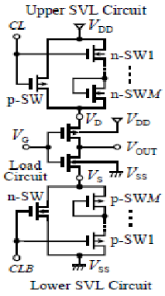

FIGURE 3.3. CIRCUIT OF SVL CIRCUIT

IV. CMOS CURRENT COMPARATOR CIRCUIT DESCRIPTION AND OPERATION:

The most signal processing applications of comparator is the detection of multiple threshold so we discuss about multiple comparator circuit configuration for example a trio of simple current comparator with outputs A,B and C are shown in figure 4.1.

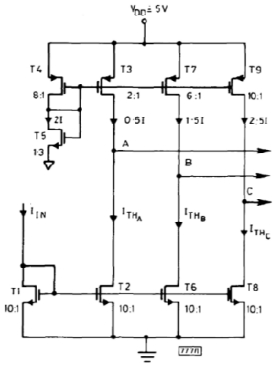

FIGURE 4.1. CIRCUIT OF SIMPLE CURRENT COMPARATOR IN TRI STATE

We will discuss the operation of comparator A where the input current Iin is applied to the drain of the transistor T1 and diode connnected. Transistor T2 reproduces this input current that is also

reproduced by T3 to establish the threshold current Ith. If the input current is less than the threshold current we want voltage Vds to be low. But we need the output voltage to fall low when the threshold current exceeds the input current for that reason transistor T1 and T2 will be operating in the saturation and linear regions.

The N-channel transistor T generates Vgs and for T1 in the saturation region

$$I_{in} = X_1(W/L)_1 (V_{gs}-V_{TH})^2 \quad -(2)$$

And for transistor T2 in the linear region

$$I_{d2}=X_2(W/L)_2(2(V_{gs}-V_{t2})V_{ds2}-V^2_{ds2}) - (3)$$

The identical Nmos transistor with identical(W/L) ratio has identical X's and Vth.To turn off the gate Vds must be low and set the maximum allowable low logic level of the output to be about one-third the NmosVth.let assume that the low value of the output voltage occurs when the input current is 1.1 times as large as the threshold cuurent. when the output becomes low by using the above two drain current equation we can solve Vgs as 1.5v.By having Vgs and input current we can solve width to length ratio of transistor T1 and T2.

V. CMOS CURRENT COMPARATOR LOGIC STYLES :

1.PSEUDO NMOS LOGIC

2.TRANSMISSION GATE LOGIC

5.1. PSEUDO NMOS LOGIC:

The invertor that uses a p-device pull up or load has its gate permanently ground. An n-device pull down or driver is driven with the input signal. This is roughly equivalent to use of a depletion load and nmos technology and is thus called "Pseudo Nmos". The circuit is used in a variety of cmos circuits. In this, pmos for most of the time will be in the linear region. So that resistance will be low and hence RC time constant is also low. When the driver is the"on" condition a constant DC current flows in the circuit. The basic cmos inverter is shown in the figure5.1.1

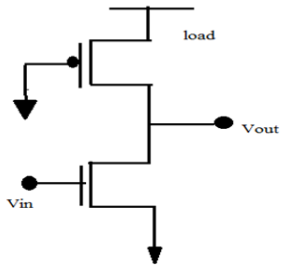

FIGURE 5.1.1.CMOS INVETER CIRCUIT

5.1.1 OPERATION:

In pseudo nmos the cmos pull up network is replaced by single pmos transistor with its gate grounded. Since the pmos is not driven by signals, it is always 'on'. The effective gate voltage seen by the pmos transistor is Vdd. Thus overall voltage on the p channel gate is always Vdd-Vtp. When the nmos is turned 'on' a direct path between supply and ground exist and static power will be drawn. However the dynamic power is reduced due to lower capacitance loading. The logic network representation of pseudonmos logic is shown in figure 5.1.2.

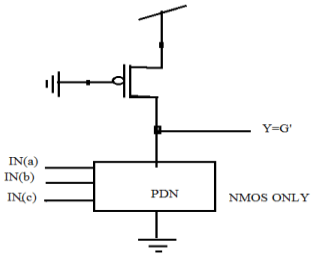

FIGURE 5.1.2.LOGIC NETWORK OF PSEUDO NMOS STYLE

The advantages of pseudo nmos is it requires less number of transistor than cmos and transmission gate style because of this advantage speed is more. This logic is also called as ratioed logic where its reduces dynamic power by reducing capacitive loading. It produces low noise margin due to high VOL. It produces non-zero static power dissipation and do not provide full output voltage swing because of pmos always 'on'. If the output is zero it has static power dissipation and if the output is non-zero it has no static power dissipation. The schematic representation of comparator using pseudo nmoslogic style is shown in figure 5.1.3 .

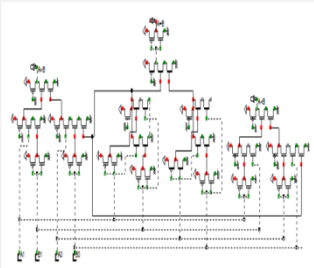

FIGURE 5.1.3.SCHEMATIC OF 2-BIT COMPARATOR USING PSEUDO NMOS LOGIC STYLE.

5.2. TRANSMISSION GATE:

A transmission gate or analog switch is defined as an electronic element that will selectively block or pass a signal from the input to the output and this switch is comprised of a pmos transistor and nmos transistor. The control gates are biased in a complementary manner so that

both transistor are ‘on’ or ‘off’. The transmission gate is also known as bidirectional switch. The common circuit symbol of the transmission gate is shown in figure 5.2.1.

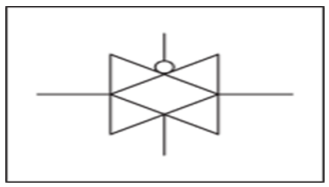

FIGURE 5.2.1. CIRCUIT SYMBOL.

5.2.1 OPERATION:

The values of p-gate and n-gate are expected to be opposite to each other. When the voltage on node A i.e., n-gate is a logic 1 the complementary logic 0 is applied to node active low A i.e., p-gate, allowing both the transistor to conduct and pass the signal at IN and OUT. When the voltage on node active low A is a logic 0,the complementary logic 1 is applied to the node A turning both the transistor off an forcing a high-impedance condition on both the IN and OUT nodes. This high-impedance condition represents the third state that the channel may reflect down stream. In all other cases drain receives an error output in which source and drain is floating. This behaviour is summarized by the following table shown below.

p-gate	**n-gate**	**Drain**
0	0	M*
0	1	SOURCE
1	0	N
1	1	M*
M/N	ANY	M*
ANY	M/N	M*

*If source is N,drain is N;otherwise drain is M.

The basic circuit of transmission gate is shown in the figure 5.2.2 and the schematic representation of the comparator using transmission gate logic style is shown in the figure 5.2.3.

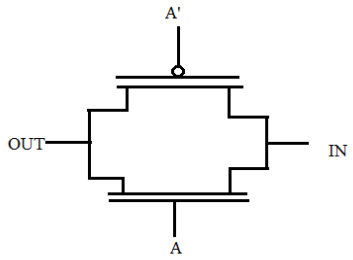

FIGURE 5.2.2.CIRCUIT OF TRANSMISSION GATE

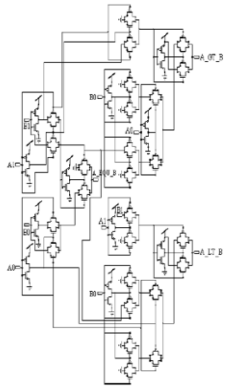
FIGURE 5.2.3.SCHEMATIC OF 2-BIT COMPARATOR USING TRANSMISSION GATE LOGIC STYLE.

VI. SIMULATION RESULT:

In this section the simulation of current comparator and the SVL modified CMOS current comparator was designed as shown in the figure 6.1 and 6.2 and 6.3. The simulation and design are obtained in the tanner tool using s-edit. The analysis of power consumption and delay are obtained using t-spice simulator. The power consumption of conventional CMOS current comparator is 258.6µw and the power consumption of SVL modified CMOS is 156.7µw where 60% of power consumption is reduced. The result shows thst SVL modified CMOS consumes less power when compared to conventional CMOS current comparator.

POWER CONSUMPTION IS 258.6µw

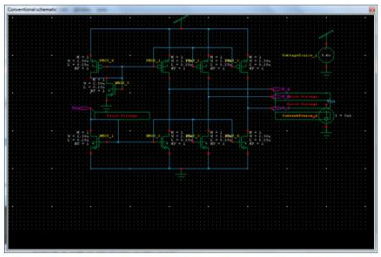

FIGURE 6.1.BASIC CIRCUIT FORCMOS CURRENT COMPARATOR

POWER CONSUMPTION IS 156.7µw

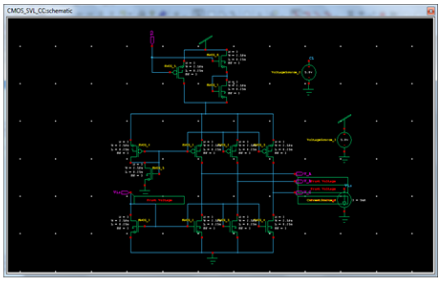

FIGURE 6.2.SVL MODIFIED CMOS CURRENT COMPARATOR

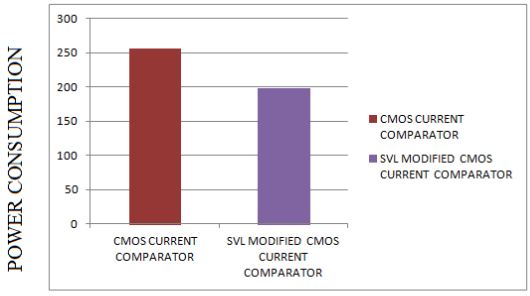

FIGURE 6.3.GRAPH FOR POWER CONSUMPTION

The simulation of CMOS current comparator with pseudo nmos logic using SVL technique is shown in the figure 6.4 and 6.5 and 6.6. The power consumption of CMOS current comparator with pseudo nmos is 248.75µw and for CMOS current comparator with pseudo nmos using SVL technique is198.50µw where 80% of power consumption is reduced. The result shows that SVL modified CMOS current comparator consumes less power.

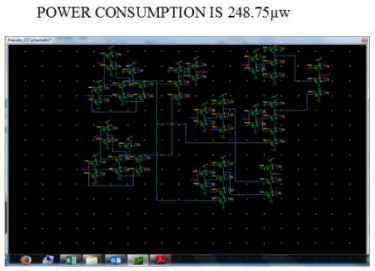

FIGURE 6.4.CMOS CURRENT COMPARATOR WITH PSEUDO NMOS LOGIC

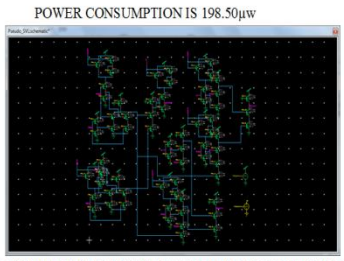

FIGURE 6.5.SVL MODIFIED CMOS CURRENT COMPARATOR WITH PSEUDO NMOS LOGIC

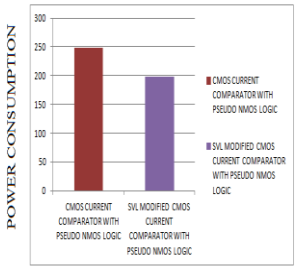

FIGURE 6.6.GRAPH FOR POWER CONSUMPTION FOR CMOS CURRENT COMPARATOR WITH PSEUDO NMOS LOGIC

The simulation of CMOS current comparator with transmission gate logic style using SVL technique is shown in the figure 6.7 and 6.8 and 6.9. The power consumption of CMOS current comparator with transmission gate logic is 435.9µw and for CMOS current comparator with transmission gate logic using SVL technique is 289.7µw where 55% of power consumption is reduced. The result shows that SVL modified CMOS current comparator consumes less power.

POWER CONSUMPTION IS 435.9µw

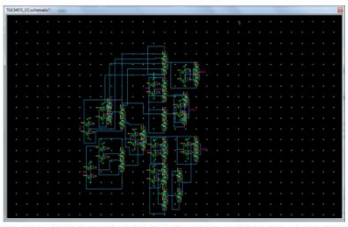

FIGURE 6.7.CMOS CURRENT COMPARATOR WITH TRANSMISSION GATE LOGIC

POWER CONSUMPTION IS 289.7µw

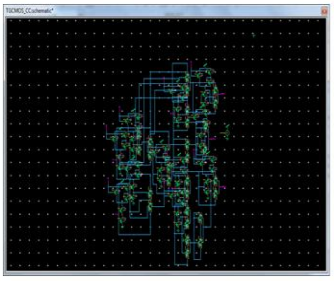

FIGURE 6.8.SVL MODIFIED CMOS CURRENT COMPARATOR WITH TRANSMISSION GATE LOGIC

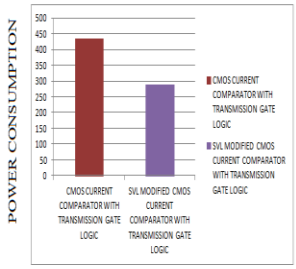

FIGURE 6.9.GRAPH FOR POWER CONSUMPTION FOR CMOS CURRENT COMPARATOR WITH TRANSMISSION GATE LOGIC

VII. CONCLUSION:

A SVL self controllable voltage level circuit with current comparator which overcomes the drawbacks of MTCMOS and VTCMOS was developed. This SVL circuit can dynamically reduce Vdsn drain to source voltage and increase the substrate bias of MOSFET which is in off condition in the stand by load circuit. After simulations of designs with pseudo nmos and transmission gate logic final results are obtained for power consumption. The result shows that Pseudo nmos logic consumes low power when compared to transmission gate logic style.

An important factor is that output voltage swing is better in cmos design and transmission gate logic style. But transmission gate requires more number of transistors when compared to cmos design style. The drawback in transmission gate can be overcome in pseudo nmos logic which requires less number of transistor. The power consumption of the current comparator with pseudo nmos and transmission gate logic using SVL circuit consumes less power when compared to normal current comparator with these logics.

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