EFFICIENT APPROACHES FOR DESIGNING THE LOGICAL REVERSIBILITY OF COMPUTATION

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Submitted: May 27, 2017 ***Accepted: June 15, 2017*** ***Published: Sep 1, 2017***

Abstract-The work demonstrates about the reversible logic synthesis for the 2 to 4 decoder, the circuits are designed using reversible fault tolerant toffoli gates. Thus the entire scheme inherently becomes fault tolerant. In addition, several lower bounds on the number of constant inputs, garbage outputs and quantum cost of the reversible fault tolerant decoder have been proposed. Transistor simulations of the proposed decoder power consumption have been reduced than the existing approach without decreasing the speed, which proved the functional correctness of the proposed Decoder. The comparative results show that the proposed design is much better in terms of quantum cost, delay, hardware complexity and has significantly better scalability. Tanner software is the advanced industrial tool that is growing up in trend. So the proposed decoder is designed in Tanner EDA after completion of the circuit in DSCH and Microwind. This shows the power dissipation and power consumption at each nook and corner to re-design with low power consumption possible.

Index terms*:* Fast Fourier Transform (FFT),:Reversible Logic Synthesis(RLS).

I. INTRODUCTION

Reversible computing is a model of computing where the computational process to some extent is reversible, i.e., time invertible. A necessary condition for reversibility of a computational model is that the relation of the mapping states of transition functionsto their successors should at all times be one-to-one. Reversible computing is generally considered an unconventional form of computing.The implementation of reversible computing thus amounts to learning how to characterize and control the physical dynamics of mechanisms to carry out desired computational operations so precisely that we can accumulate a negligible total amount of uncertainty regarding the complete physical state of the mechanism, per each logic operation that is performed. In other words, we would need to precisely track the state of the active energy that is involved in carrying out computational operations within the machine, and design the machine in such a way that the majority of this energy is recovered in an organized form that can be reused for subsequent operations, rather than being permitted to dissipate into the form of heat. Although achieving this goal presents a significant challenge for the design, manufacturing, and characterization of ultraprecise new physical mechanisms for computing, there is at present no fundamental reason to think that this goal cannot eventually be accomplished, allowing us to someday build computers that generate much less than 1 bit's worth of physical entropy (and dissipate much less than kT in 2 energy to heat) for each useful logical operation that they carry out internally. Reversible logic circuits have been historically motivated by theoretical research in low power electronics as well as practical improvement of bit manipulation transforms in cryptography and computer graphics. Recently, reversible circuits have attracted interest as components of quantum algorithms, as well as in photonic and nano computing technologies where some switching devices offer no signal gain. Research in generating reversible logic distinguishes between circuit synthesis, post synthesis optimization, and technology mapping. In this survey, we review algorithmic paradigms search based, cycle based, transformation based, and BDD based as well as specific algorithms for reversible synthesis, both exact and heuristic. We conclude the survey by outlining key open challenges in synthesis of reversible and quantum logic, as well as most common misconceptions.

II. LITERATURE SURVEY

A computation is reversible if it can be 'undone' in the sense that the output contains sufficient information to reconstruct the input, i.e., no input information is erased . It is also common to require that no information is duplicated. In Computer Science, reversible transformations have been popularized by the Rubik's cube and slid ingtile puzzles, which fueled the development of new algorithms, such as iterative deepening A search Prior to that, reversible computing was proposed to minimize energy loss due to the erasure and duplication of information[1,2].Today, reversible information processing draws motivation from several sources. Considerations of power consumption prompted research on reversible computation, historically. In 1949, John Von Neumann estimated the minimum possible energy dissipation per bitas k_BT ln 2 where k_B = 1:38065 × 10^{-23}J=K is the Boltzmann constant and T is the temperature of environment. Subsequently, Landauer pointed out that the irreversible erasure of a bit of information consumes power and dissipates heat. While reversible designs avoid this aspect of power dissipation, most power consumed by modern circuits is unrelated to computation but is due to clock networks, power and ground networks, wires, repeaters, and memory. A recent trend in low power electronics is to replace logic reversibility by charge recovery, e.g., through dual rail encoding where the 01 combination represents a logical 0 and 10 represents a logical 1[3,4].

Signal processing, cryptography, and computer graphics often require reversible transforms, where all of the information encoded in the input must be preserved in the output. A common example is swapping two values a and b without intermediate storage by using bitwise XOR operations a = a+b, b = a+b, a = a+b. Given that reversible transformations appear in bottlenecks of commonly used algorithms, new instructions have been added to the instruction sets of various microprocessors such as v perm in PowerPC AltiVec, bshuffle in Sun SPARC VIS, permute and mix in HP PARISC, pshufb in Intel IA32 and mux in Intel IA64 to improve their performance . In particular, the performance of cryptographic algorithms DES, Two fish and Serpent, as well as string reversals and matrix transpositions, can be considerably improved by the addition of bit permutation instructions . In another example, the reversible butterfly operation is a key element for Fast Fourier Transform (FFT) algorithms and has been used in application specific Xtensa processors from Tensilica. Reversible computations in these applications are usually short and hand optimized[5,6].

Program inversion and reversible debugging generalize the 'undo' feature in integrated debugging environments and allow reconstructing sequences of decisions that lead to a particular

outcome. Automatic program inversion and reversible programming languages allow reversible execution. Reversible debugging supports reverse expression watch pointing to provide further examination of a problematic event[7].

Networks on chip with mesh based and hyper cubic topologies perform permutation routing among nodes when each node can both send and receive messages. To route a message, regular permutation patterns such as bit reversal, complement and transpose are applied to minimize the number of communication steps. Nano and photonic circuits are made up of devices without gain, and they cannot freely duplicate bits because that requires energy. They also tend to recycle available bits to conserve energy. Generally, building nano size switching devices with gain is difficult because this requires an energy distribution network. Therefore, reversibility is fundamentally important to nano scale computing, although specific constraints may vary for different technologies. Quantum computationS is another motivation to study reversible computation because unitary transformations in quantum mechanics are reversible. Quantum algorithms have been designed to solve several problems in polynomial time, where best known conventional algorithms take more than polynomial time. A key example is number factoring, which is relevant to cryptography. While unitary transformations can be difficult to work with in general, many prominent quantum algorithms contain large blocks with reversible circuits that do not invoke the full power of quantum computation, e.g., for arithmetic operations. Circuits for quantum error correction contain large sections of reversible circuits that implement GF linear transformations .

III. PROPOSED SYSTEM

Decoders are the collection of logic gates fixed up in a specific way such that, for an input combination, all outputs terms are low except one. These terms are the minterms. Thus, when an input combination changes, two outputs will change. Let, there are n inputs, so number of outputs will be 2n. There are several designs of reversible decoders in the literature. To the best of out knowledge, the designs from is the only reversible design that preserve parity too.

1.1 Feynman Double Gate:

The input vector is I (A, B,c) and the output vector is O (P, Q,R). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 2. Input vector (Iv) and output vector (Ov)

for 3 × 3 reversible Feynman double gate (F2G) is defined as Iv = (a, b, c) and Ov =(a, a ⊕ b, a ⊕ c) shown in fig 1 and indicated in table 1.

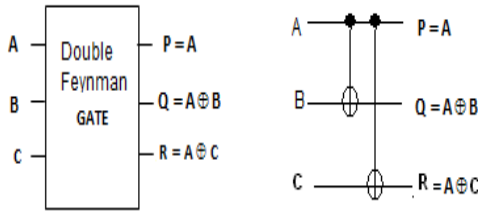


Fig.1. Feynman double gate

Table.1. Truth Table of Feynman Double Gate

INTPUT			OUTPUT		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

1.2 Fredkin Gate:

The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5. The input and output vectors for 3 × 3 Fredkin gate (FRG) are defined as Iv = (a, b, c) and Ov = (a, a_b ⊕ ac, a_c ⊕ ab). To realize the FRG, four transistors are needed shown in fig 2 and indicated in table 2.

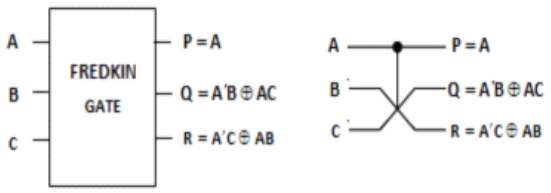


Fig.2. **3x3 Fredkin gate**

Table.2.Truth Table Of Fredkin gate

INTPUT			OUTPUT		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

1.3 Toffoli Gate:

The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5shown in fig 3 and indicated in table 3.

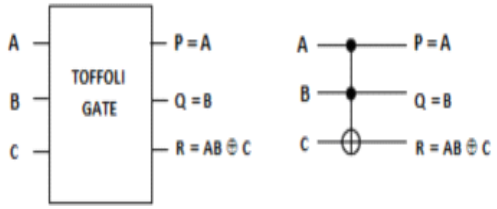


Fig.3.Toffoli Gate

Table.3.Truth Table Of Toffoli Gate

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	1	0

1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

The reversible logic is being used with Toffoli gate which is also a reversible gate. Toffoli gate consists of many small combinational gates such as AND, OR gates which are connected together to form decoder. These gates can be externally connected together for separate purpose. The idea seems to be like a cellphone used for multi-tasking purpose like talk, listen to music, games etc. The power consumption is much reduced to greater extent. Decoder may produce error bits in the output due to many problems.These gates are embedded in the same decoder block. Whatever gates are required that can be used and other gates are left as it is. This is done by power grating method. In this method, only the required gates are taken into account while others are left as it is with switching technique with the VDD and GND for the active circuit. But for the circuit to act as the complete decoder, all the Toffoli gates are taken into use. Again if a number of the gates are used, then the power consumption may increase in this method. But this is reduced by giving the inputs to each of the gates by bypassing the inputs. There is no need of the method application in the encoder as encoding is to encode the check bits to the input. So there is no need of the reversible logic over there. The fault tolerant can be used in all the power low usage devices. It is mainly used in digital image processing, networking etc.So in our work, the toffoli decoder is designed in such a way that four toffoli individual gate is grouped together to form decoder as a whole while individually they contribute to the individual AND gates. In this way, the proposed circuit can operate as both decoder and the individual operation that is required which was not possible in previous proposals.At the same time reducing the garbage outputs to maximum extent possible. Another criteria that has to be taken into account is the power consumption is the reason for the design of the project. The power consumed in Toffoli decoder is very much reduced than fredkin and freymann gates described in our work. The speed of the decoder doesn't get affected due to the multiple operation as the operation is parallel processing and the delay of the circuits are reduced to the minimum value.The area occupied by the decoder is also less i.e the range is in micrometers as the transistor sizing is made to nanometers. The designed decoder will reduce the area consumption without retarding the speed.

The designed decoder also will correct the bit loss which is prominent in communication systems. There always occurs bit loss problem while sending the information from transmitter to receiver. The decoder is designed till now is designed with parity checker. So in our designed decoder the bit loss is removed by the toffoli gate logic. The logic is that p=a,q=b and r=(ab)xor(c) where a,b and c are the inputs while p,q ,r are the outputs. So the bit loss can easily be recovered by this logic by the first two logicshown in fig 4 . So this proves to be advantageous in our design.Tanner technology is mainly used in determining the substrate transistor width, transistor length, cut-off frequency etc. Tanner software is the industrial tool that is growing up in trend. So the proposed decoder is designed in Tanner EDA after completion of the circuit in DSCH and Microwind. Tanner is the advanced industrial tool which shows the power dissipation and power consumption at each nook and corner to re-design with low power consumption possible

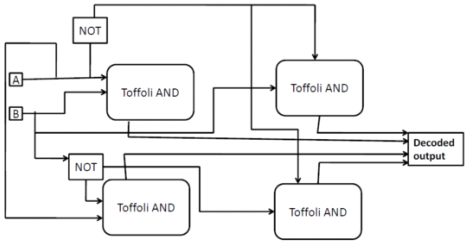


Fig.4.Block Diagram of Reversible Fault Tolerent

Decoder

Let us suppose that a logic network has 2 inputs A and B. They will give rise to 4 states A, A', B, B' . The truth table for this decoder is shown below table 4,5&6.

Table4.TruthTableof2:4decoders

INPUT			OUTPUT			
A	B	C	O0	O1	O2	O3
0	0	0	0	0	0	1
0	1	0	0	0	1	0
1	0	0	0	1	0	0
1	1	0	1	0	0	0

0	0	1	1	1	1	0
0	1	1	1	1	0	1
1	0	1	1	0	1	1
1	1	1	0	1	1	1

S_1	S_0	E	O_0	O_1	O_2	O_3
×	×	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

Table.5.Truth Table of Proposed Decoder

Table.6.Truth Table of Reusable Decoder

INPUT				OUTPUT				
A	B	C	Control Switch	O 0	O 1	O 2	O 3	AN D
0	0	0	0	0	0	0	1	0
0	1	0	0	0	0	1	0	0
1	0	0	0	0	1	0	0	0
1	1	0	0	1	0	0	0	0
0	0	1	1	1	1	1	0	1
0	1	1	1	1	1	0	1	1
1	0	1	1	1	0	1	1	1
1	1	1	1	0	1	1	1	1

IV. EXPERIMENTAL RESULTS

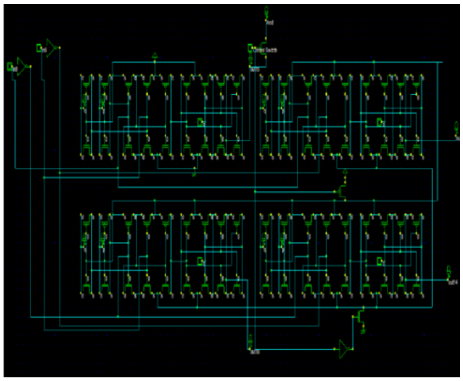


Fig.5.Schematic Diagram of Decoder

Fig.6Timing Diagram Of Decoder

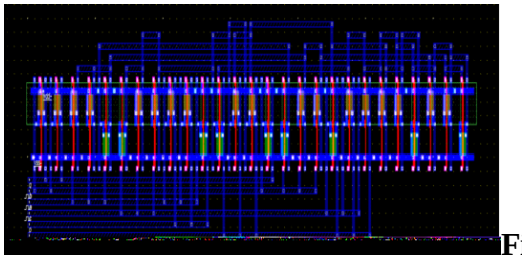


Fig.7 Layout Diagram Of Proposed Decoder

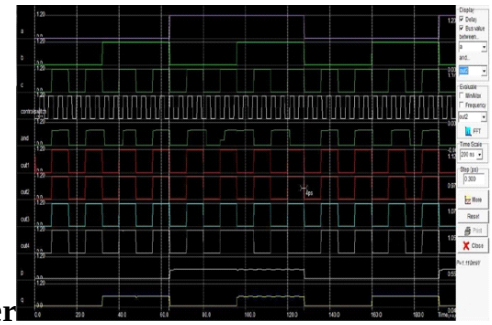


Fig 8.Analog Simulation Result

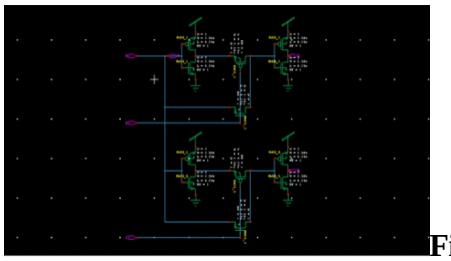


Fig.9Schematic Diagram of Feynman Double

Gate

Fig.10. Schematic Diagram of Fredkin Gate

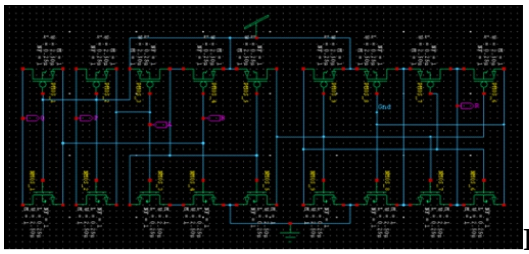
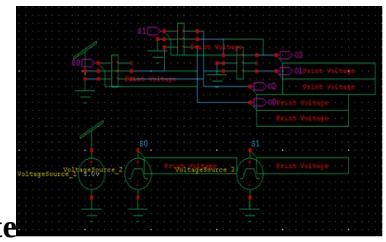
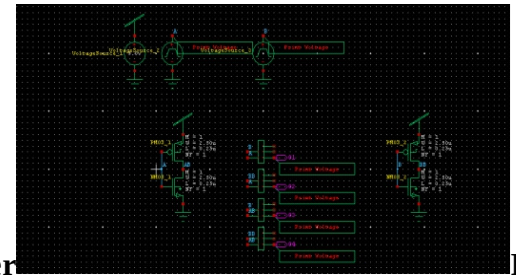


Fig 11. Schematic Diagram of Toffoli



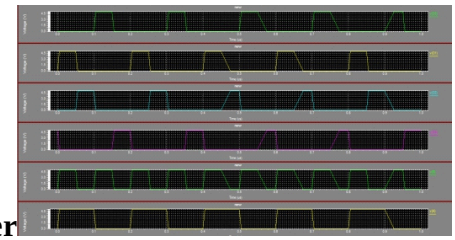
Gate

Fig.12 Schematic Diagram of Existing Fault Tolerent



Decoder

Fig.13 Schematic Diagram of Proposed



Fault Tolerant Decoder

Fig 14 Simulation result of existing decoder

Fig 5 shows the schematic diagram of the proposed fault tolerant decoder in DSCH. This circuit consists of four toffoli gates connected together to form the decoder. The inputs given a and b. The input c is given to each of the toffoli gate separately. The And output is obtained with control switch switched on and depending on the inputs Fig 6 shows the timing diagram of the proposed fault tolerant decoder in DSCH. The inputs are given with control switch and the outputs are observed. The out1, out2, out 3 and out 4 are the decoder outputs while p and q are the outputs as per toffoli logic. The AND gate output switches on with both the inputs a and b on and enabling the control switch. Fig.7 shows Layout Diagram of Proposed Fault Tolerent Decoder drawn in the microwind with the help of the schematic drawn in DSCH.

Fig.9 shows the circuit diagram of feynman double gate. This is the single Feynman gate shown in the existing system.Fig.10 shows circuit diagram of fredklin gate drawn in Tanner and compared with the Feynman double gate in the existing system. Fig.11 shows circuit diagram of a single toffoli gate which has about 9 PMOS and 9 NMOS.Fig.12 shows circuit diagram of existing fault tolerent decoder drawn in Tanner EDA with the supply voltages and inputs. Fig.13 shows circuit diagram of proposed fault tolerant decoder in Tanner EDA. Its toffoli gate is been converted into symbols by the use of Update Symbol. So the circuit is made simpler by this and the power consumption can be drastically reduced. Fig14 shows simulation result of existing decoder. The simulation result has more delay when compared with the proposed decoder. Fig15 shows the simulation result of proposed decoder which proves lower delayand the comparsion table shoiwn in table 7.

Table 7.POWER COMPARISON TABLE

DESCRIPTION	EXISTING FAULT TOLERENT DECODER	PROPOSED FAULT TOLERENT DECODER
Vdd Gnd From	0 to $1e^{-006}$	0 to $1e^{-006}$

Time		
Max Power	2.564968e-002 at time 2.2058e-009	1.231657e-003 at time 3.55e-007
Min Power	1.559627e-009 at time 0	5.781481e-009 at time 0
Average Power Consumed	1.797103e-003 watts	8.482144e-005 watts
Parsing	0.01 seconds	0.02 seconds
Setup	0.02 seconds	0.04 seconds
DC Operating Point	0.00 seconds	0.04 seconds
Transient Analysis	0.16 seconds	0.23 seconds
Overhead	6.47 seconds	6.41 seconds
Total	6.67 seconds	6.73 seconds

V. CONCLUSION

The design methodologies of an 2 to 4 reversible fault tolerant decoder. In this work we presented design methodologies of a reversible fault tolerant decoder using dsch and microwind. In this proposed circuit has been constructed with the help of reversible toffoli logic gate and it has been shown that the transistor implementation of the decoder works correctly. We proposed several

lower bounds on the numbers of garbage outputs, constant inputs and quantum cost and proved that the proposed circuit has constructed with the optimum garbage outputs, constant inputs and quantum cost.In addition, we presented the designs of the individual gates of the decoder using MOS transistors in order to implement the circuit of the decoder with transistors. Simulations of the transistor implementation of the decoder showed that the proposed fault tolerant decoder works correctly. The comparative results proved that the proposed designs perform better than its counterpart. We also proved the efficiency and supremacy of the proposed scheme with several theoretical explanations. Proposed reversible fault tolerant decoders can be used in parallel circuits, multiple-symbol differential detection network components and in digital signal processing etc.

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