DESIGN AND FPGA IMPLEMENTATION OF NON-LINEARITY COMPENSATION OF CAPACITIVE PICK-OFF MEMS ACCELEROMETER FOR SATELLITE LAUNCH VEHICLES

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Abstract- This paper presents the algorithm on the compensator design for eliminating the non-linearity in the capacitive pick-off MEMS open-loop accelerometer and its implementation in the FPGA. A simple and elegant method is presented for the purpose. In the sensor model of compensator, upto 3rd order terms are taken. The first step approximation is derived using linear model. This approximation is improved over iterations to reduce the non-linearity. With this method, the inertial navigational grade performance is achieved. The algorithm is coded in VHDL, simulated, synthesized and implemented in the FPGA and tested. Test results matches closely with that of simulations. The VHDL design can be easily targeted into an ASIC to realize an integrated smart sensor.

Index terms: Accelerometer, Linearity, FPGA, error compensation