Vedic Mathematics Based 32-Bit Multiplier Design for High Speed Low Power Processors

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Abstract- Vedic Mathematics is the ancient methodology of Indian mathematics which has a unique technique for arithmetic computations based on 16 Sutras (Formulae). Transistor level implementation (ASIC) of Vedic Mathematics based 32-bit multiplier for high speed low power processor is reported in this paper. Simple Boolean logic is combined with 'Vedic' formulas, which reduces the partial products and sums generated in one step, reduces the carry propagation from LSB to MSB. The implementation methodology ensure substantial reduction of propagation delay in comparison with Wallace Tree (WTM), modified Booth Algorithm (MBA), Baugh Wooley (BWM) and Row Bypassing and Parallel Architecture (RBPA) based implementation which are most commonly used architectures. The functionality of these circuits was checked and performance parameters like propagation delay and dynamic power consumption were calculated by spice spectre using standard 90nm CMOS technology. The propagation delay of the resulting 32×32 multiplier was only ~1.06 us and consumes ~132 uW power. The implementation offered significant improvement in terms of delay and power from earlier reported ones.

Index terms*:* Vedic Formulae, Multiplication, High Speed, Low Power, Latency.