0.35 µm CMOS OPTICAL SENSOR FOR AN INTEGRATED TRANSIMPEDANCE CIRCUIT

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Abstract- This paper presents an integrated optical receiver which consists of an integrated photodetector, and a transimpedance circuit. A series inductive peaking is used for enhancing the bandwidth. The proposed structure operates at a data rate of 10 Gb/s with a BER of 10^{-20} and was implemented in a 0.35 µm CMOS process.

The integrated photodiode has a capacitance of 0.01 pF which permits to the structure to achieve a wide bandwidth (5.75 GHz) with only one inductor before the last stage; hence a smaller silicon area is maintained. The proposed TIA has a gain of 36.56 dBΩ (67.57 KΩ), and an input courant noise level of about 25.8 pA/$Hz^{0.5}$. It consumes a DC power of 87.4 mW from 3.3 V supply voltage.

Index terms: CMOS technology, Integrated photodiode; SML photodiode; Transimpedance, bandwidth enhancement; shunt and series peaking;

I. INTRODUCTION

The recent rapid progress of data transportation volume and speed has brought great demands of high bandwidth, low cost and low power integrated optical communication circuits [1]. A high speed optical receiver generally consists of a photodiode, a transimpedance amplifier (TIA) and a limiting amplifier (LA). The TIA, which converts and amplifies the induced photo current into voltage for following signal processing, must has a large bandwidth to support high-bit rate applications. In the design of a low cost and low power TIA for optical communication system, deep sub-micron CMOS technology is the primary candidate for its low cost and easy of fully-integration [1-4].

The major difficulty in designing the wideband TIA lies in the large natural photodiode capacitance at the input node. Therefore, different techniques are introduced to extend bandwidth. Many techniques, such as inductive-series peaking, passive network input matching and inductive shunt peaking, have been proposed to solve this problem. However, most of these techniques require several inductors, which occupy large silicon areas and may introduce undesired interferences to other circuits.

This paper describes the design of a fully integrated optical receiver that operates at a data rate of 10 Gbps. The next section of the paper focuses on CMOS integrated photodetectors. Then, we show implementation of CMOS transimpedance amplifier and conclude this paper with the simulation's results.

II. INTEGRATED PHOTODETECTORS

When a burst of photons arrives at the surface of the photodetector, a fraction of the optical power is absorbed by the material and decays exponentially as a function of the penetration depth. As the field propagates into the material, it is attenuated and some of its energy is used to excite electron-hole pairs into the conduction and valence bands respectively. To harness these photo-generated charge carriers they have to be separated by an electric field before they recombine. These accelerated electron-hole pairs then give rise to a photocurrent that can be processed by the remaining optical receiver circuitry.

A. Photodetector structures in CMOS

If a photodetector is to be implemented in a standard CMOS process the photo-generated charge carriers have to be accelerated by electric fields that exist within the material. Significant electric fields are present in the depletion regions formed at all pn junctions and can be used to harvest electron-hole pairs. Fig. 1 illustrates the basic structures present in a standard CMOS process [16].

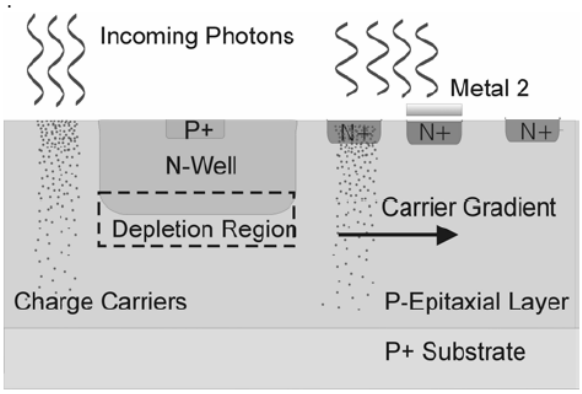


Fig. 1. Photo-detection structures available in a standard CMOS process.

Incoming photons excite charge carriers within the substrate. An important design parameter that has to be considered when selecting a structure is the responsivity of the photodetector. Responsivity is a measure of the current that is generated for a given optical input power and is proportional to the pn junction's quantum efficiency.

Even though detector responsivity is an important design parameter, it is the slow detector response times that have been found to prevent the implementation of fully integrated

CMOS-based receivers. Electron-hole pairs that are generated deep within the substrate and have to diffuse a considerable distance to reach the depletion region slow down the photodetector impulse response and result in a low frequency current gain. The effect of this diffusion tail is to increase the amount of inter symbol interference (ISI) between consecutive light pulses, resulting in an increased bit error rate.

B. Spatially modulated detector structures

To minimize the effect of this diffusion current on the detector frequency response, a spatially modulated light (SML) detector was implemented by placing a grid of identical pn junctions onto the

silicon surface and then masking alternate ones with a floating metal layer [2]. When this detector is illuminated, the absorbed light creates a spatial gradient in the carrier concentration that will relax by diffusion. The difference between illuminated and masked current responses will then result in an equivalent drift current response component that minimizes the diffusive tail. A spatially modulated light detector using the pn-junction formed between the n+ and p- epitaxial layer substrate was found to be the only structure in the CMOS process that could accommodate the high data-rate required. As the frequency response of a CMOS photo-detector is mainly determined by the transport of minority carriers [2].

As the SML structure uses the relaxation of the gradient to extract information from the incoming burst of photons, the data rate that can be supported is much higher than can be realized with other CMOS photo-diode structures.

C. Photodetector in AMS 0.35µm CMOS

In order to achieve high-speed performance, such as that required for several GHz applications, whilst catering for the commercial AMS CMOS 0.35 µm technology with no process modification, we have taken the approach mentioned previously of treating the n-well in standard CMOS process as a screening terminal to block the slow bulk carriers [3]. SML-detector [5] is an other potential candidate which also trades responsivity for speed, but it necessitates the differential system architecture, while in our optical front end system, stringent power consumption requirement prefers the single-ended implementation.

A sketch of the fabricated detector structure is shown in Fig. 2. The n-well in which the detector was made forms the active region that senses the incident light. The p+, n+ diffusion forms the anode and cathode of the photodiode, and are interdigitated with a separation width of s. The width w of p+ diffusion was chosen to have the smallest value based on the design rules in order to minimize the collection time of the photogenerated carriers, but tradeoffs exist since a smaller w leads to larger parasitic resistance of the p+ electrodes. The separation width, s, degrades speed because of the increased traveling time for the carriers through depletion region, while smaller s induces the risk of punch through with the high reverse bias voltage across the photodiode. Two versions of photodiodes with different values of w and s have been fabricated intending to find optimum values.

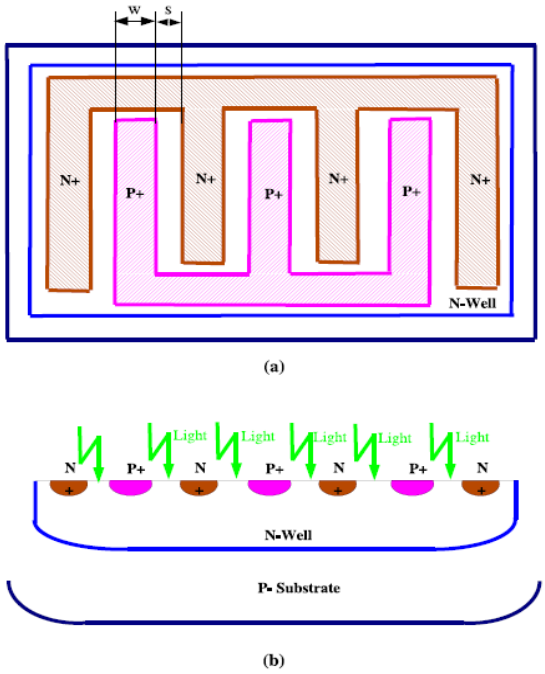


Fig. 2. Photodiode implemented in AMS C35 (a) top view of the interdigitated photodiode (b) crossection of the photodiode.

For AMS CMOS 0.35 µm technology, the p-substrate effective doping level N_{sub} is $212x10^{15}cm^{-3}$, n-well effective doping level N_{well} is $101x10^{15}cm^{-3}$, the shallow junction p+ inside n-well has an impurity concentration N_p of $3.3x10^{19}cm^{-3}$ [17, 18]. Since the desired photodiode 3 is formed by the junction between p+ and n-well, N_p and N_n have the values of $3.3x10^{19}cm^{-3}$, $101x10^{15}cm^{-3}$.

$$\phi_i = \frac{KT}{q}\lg\left(\frac{N_n.N_p}{N_i^2}\right) = 0.96\text{V} \quad (1)$$

With the junction potential known, the total width of the depletion region of an applied reverse bias voltage ΔV of 3.3 V can be derived from equation 2 :

$$x_d = x_n + x_p = \sqrt{\frac{2\varepsilon_0\varepsilon_i}{q}\left(\frac{1}{N_n}+\frac{1}{N_P}\right).(\Delta V + \phi_i)} = w_{d0}\sqrt{1+\frac{\Delta V}{\phi_i}} \approx 0.23\mu\text{m} \quad (2)$$

where x_n and x_p are the junction depths from the metallurgical junction on the n-type material and p-type material respectively. ε_0 is the dielectric constant in vacuum ($8{,}85 * 10^{-12}\mathrm{F/m}$), ε_i is the relative dielectric constant of the semiconductor, here 11,7 for silicon, w_{d0} is the width of the depletion region with zero bias.

The capacitance of the reverse biased p-n junction is given by:

$$C_d = \varepsilon_0 \varepsilon_i \frac{A}{X_d} = \varepsilon_0 \varepsilon_i \frac{A}{w_{do}\sqrt{1+\frac{\Delta V}{\phi_i}}} \quad (3)$$

where A is the junction area. Fig. 3 indicates that the junction capacitance is dependent on the reverse bias voltage. As shown, it is desirable to work at higher reverse bias voltage. However, the maximum reverse bias voltage is limited by the break down potential of the photodiode. Since higher doping level lowers the break down voltage [6], this makes the shallow junction based photodiode vulnerable.

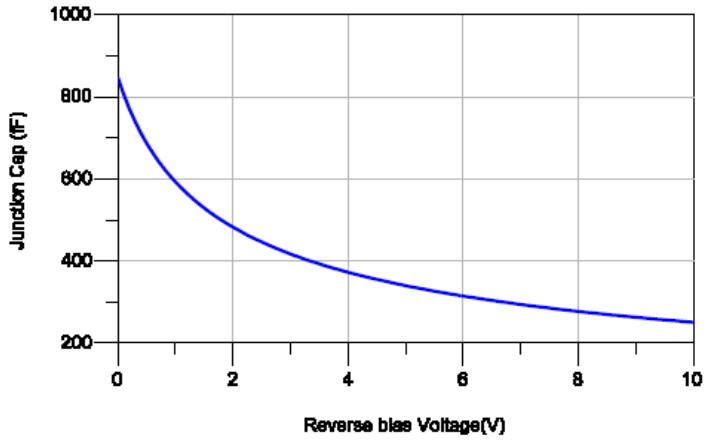


Fig. 3. Junction capacitance vs. reverse-bias voltage for the chosen CMOS technology

Assuming that the area of the photodiode is 30µm * 30µm, with a reverse bias voltage of 3.3V, the junction capacitance of the diode is :

$$C_d = \varepsilon_0 \varepsilon_i \frac{A}{X_d} = 8{,}85 * 10^{-12}.11{,}7 * \frac{13{,}6*10^{-6}*16{,}6*10^{-6}}{0{,}23*10^{-6}} \approx 0.1\ \mathrm{pf}$$

Based on previous hand calculations and simulation results, a photodiode have been fabricated in AMS 0.35 mm CMOS process, which are shown in Fig. 4. The area of this photodiode is 225.76 µm^2.

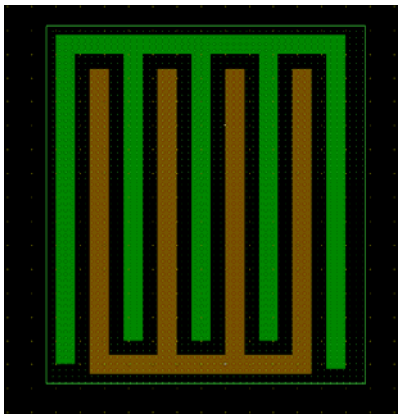


Fig. 4. 0,35µm CMOS photodiode Layout

III. TRANSIMPEDANCE AMPLIFIER

The purpose of the preamplifier stage is to convert a miniscule photocurrent into a usable voltage, and several solutions exist for achieving this goal. Prior to the transimpedance amplifier, common solutions were to use either a low impedance or high impedance open-loop voltage amplifier, and convert the photocurrent to an input voltage using a resistor to ground. There are pros and cons for each topology, but the transimpedance amplifier suits us well due to its high bandwidth and high transimpedance gain.

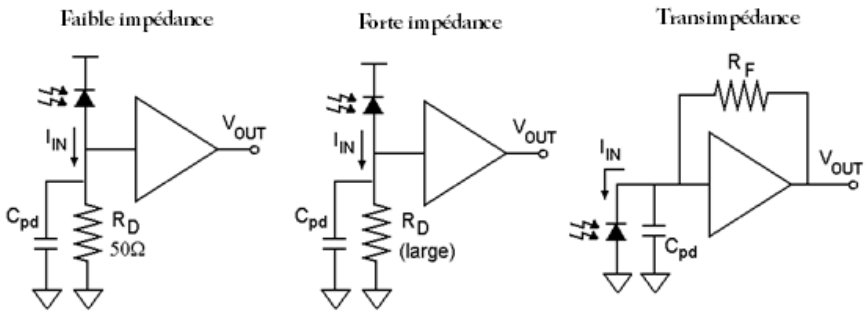


Fig. 5. Preamplifier configuration

The transimpedance amplifier (TIA) is the most common implementation of the preamplifier circuit for high-speed optical receivers. Merits for using transimpedance amplifiers include its ability to couple

a relatively large transimpedance gain with high bandwidth. These two factors directly relate to sensitivity of the detection circuit and its speed respectively. Transimpedance amplifiers are efficient at converting trivial currents produced by the photodiode to considerable voltages that can be fed to decision making logic circuits. The transimpedance amplifier can be viewed as a single ended voltage amplifier with a single feedback resistor providing current feedback. The high input resistance of the voltage amplifier is now replaced with the feedback resistance, which is lowered by A, the open-loop voltage gain. We have used a PMOS device in its linear region for the feedback resistance in order to avoid process variation problems with an ohmic resistor.

The overall transimpedance gain and bandwidth of the preamplifier system is:

$$\frac{V_{OUT}}{I_{in}} = -R_F \frac{A}{(1+A)+s\,R_F\,C_{in}} \approx -R_F \frac{1}{1+s\left[\frac{R_F\,C_{in}}{1+A}\right]} \tag{4}$$

$$f_{3dB} = \frac{1+A}{2\pi\,R_F\,C_{in}} \tag{5}$$

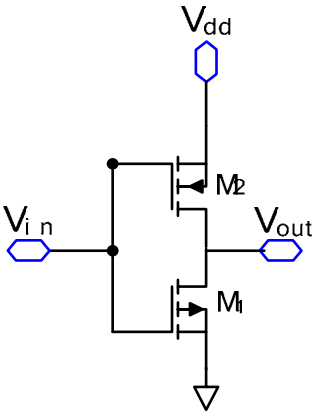
For sufficiently high A, the transimpedance gain is simply the feedback resistance. The cutoff frequency of the closed-loop response is directly related to the open-loop voltage gain of the system. Therefore, we want to maximize the open-loop voltage gain of the system. The dominant pole of the system is due to the diode capacitance, and the feedback resistance, which must be balanced to simultaneously maximize the system transimpedance gain and bandwidth.

The value of the photodiode capacitance must be low to increase the bandwidth of the amplifier. However, the low input impedance of the topology reduces this capacitive effect and allows for enlargement of the transmission capability.

If the feedback resistor is implemented with a MOS transistor in the triode region, its value can be continuously adjusted via the gate voltage of the device. A PMOS device takes up less area for the same resistance value. However, in an n-well process, the capacitance associated to the well limits the maximum attainable bandwidth. For this reason, n-channel transistors were used in the proposed configurations. If necessary, a polysilicon resistor in parallel with the transistor can be used in order to improve linearity and limit maximum resistance.

IV. DESIGN AND IMPLEMENTATION OF A TIA

Careful selection of the open-loop voltage amplifier topology is necessary for maximizing the Transimpedance Bandwidth product. We compared several open-loop topologies before selecting the Push-Pull inverter. This configuration looks like a digital inverter, but the transistor gates are biased so that the transistors are in saturation. At this bias point the inverter is in its high-gain region. An additional advantage to this topology is the self-biasing nature of the circuit. The feedback resistor couples the DC voltage at the output back to the input, and the inverter automatically sets itself up to be in the high-gain region. The Push-Pull inverter offers a high gain, high bandwidth, and medium noise performance when compared to other topologies.



$$A_{open-loop} = -\frac{V_{out}}{V_{in}} = -\frac{g_{m1} + g_{m2}}{\frac{1}{R_{ds1}} + \frac{1}{R_{ds2}}}$$

Fig. 6.a Push-Pull inverter configuration

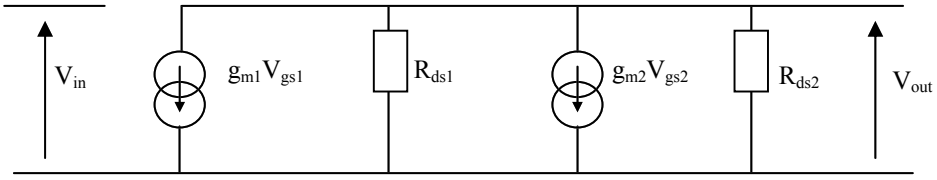


Fig. 6.b Push-Pull inverter equivalent circuit

A. Improved Design

The project specification was easily met with the 3-transistor design (2 transistors for the inverter, 1 for the feedback resistance). We took it upon ourselves to create an Improved design for the purpose of further increasing the transimpedance-bandwidth product.

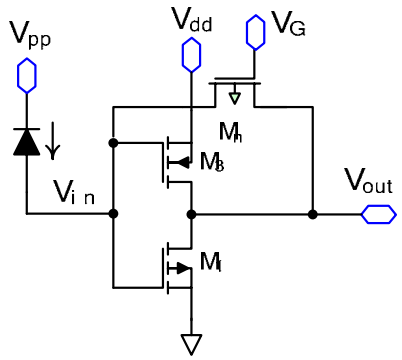


Fig. 7. Original 3-Transistor design for preamplifier stage

To obtain a high open-loop gain, the voltage amplifier in the present paper is implemented with a cascade of five stages, as depicted in Figure 8.

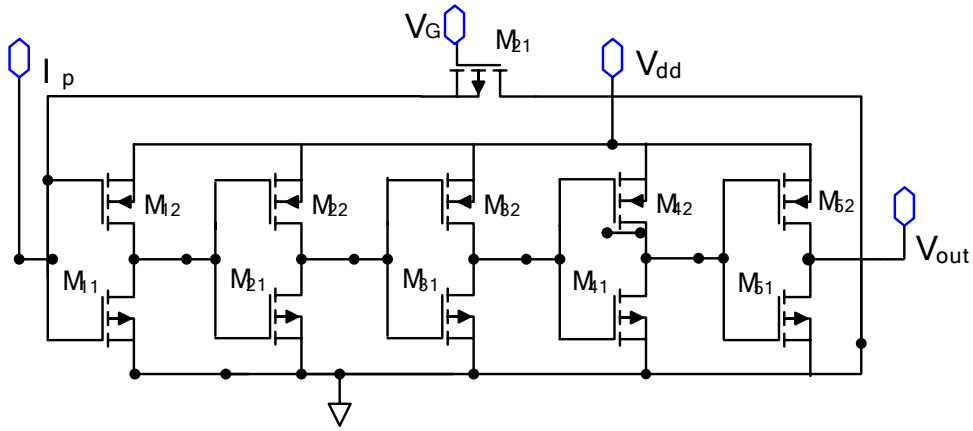


Fig. 8. The CMOS transimpedance amplifier without series peaking TIA optimization

To increase the bandwidth of an amplifier, it is important to identify the key component that is responsible for limiting the bandwidth. To have a broadband characteristic for the given amplifier and to improve the bandwidth, the shunt or series inductive peaking techniques (peak current) are generally applied. This involves placing an inductor in parallel or in series with a capacitive load; it creates a resonant circuit that draws more current in the load capacity. In extending the bandwidth results in a peak in frequency response.

Based on "series peaking" technique, we proposed the TIA structure given below. We used inductors which are inserted between stages to optimize the BW as shown in Figure 9.

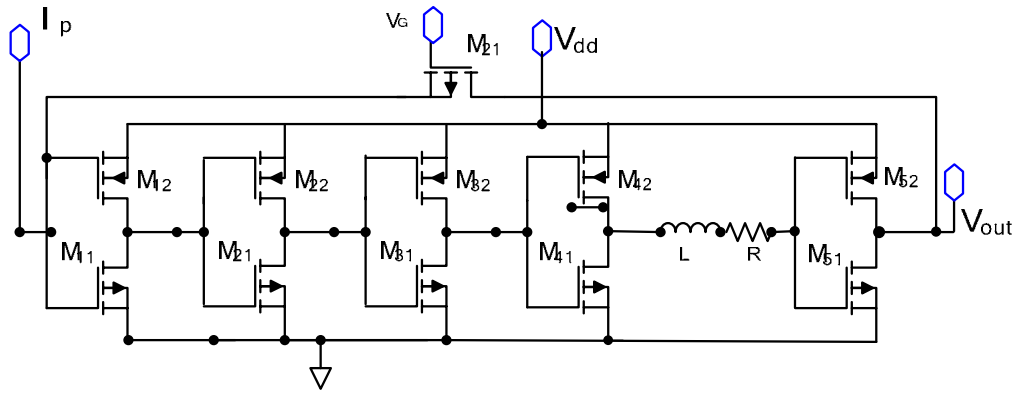


Fig. 9. The Enhanced CMOS transimpedance amplifier

The inductor in series absorbs the parasitic capacitance increase bandwidth, and decrease the courant noise.

V. SIMULATION RESULTS

All post-layout simulation results have been performed using the R_F transistor models of BSIM3v3.1, based on AMS 0.35 µm CMOS process. The table .I gives the simulation's results for the two TIA structures.

TABLE I. Simulation results of the two structures

Characteristics	Basic	Optimized
Transimpedance gain	36.56	36.56
Bandwidth (GHz)	4	5.75
Input Referred Noise	33.8	25.8
Power consumption	87.4	87.4
Bit Rate (Gb/s)	6.6	10

The improved structure exhibits a transimpedance gain (see Figure 10.) of 67.57 kΩ (36.56 dBΩ). The simulated noise at the input is depicted in Figure 11, which shows a maximum at low frequencies, then it falls and tends to zero at high frequencies along the desired frequency range.

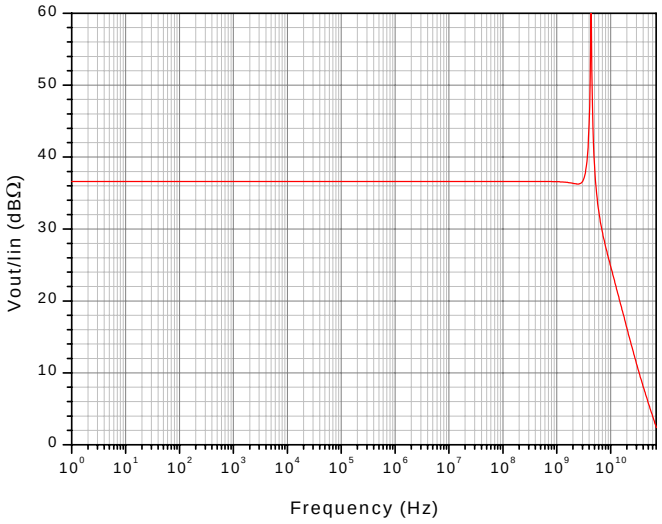


Fig. 10. The transimpedance gain of the preamplifier.

The TIA has an input current noise equal to 25.8 pA/Hz$^{0.5}$. The photodetector has a low sensitivity of 0.05 A/W, and a capacitance of 0.01 pF.

A DC analysis giving the output voltage swing as a function of the photocurrent is shown in Fig. 12. This characteristic shows a good linearity of the amplifier as well as a high dynamic range along a high input current range. We easily see that optimized structure gives the best dynamic range, and allows the detection of a photocurrent ranging from 0.5 µA to 6,2 mA.

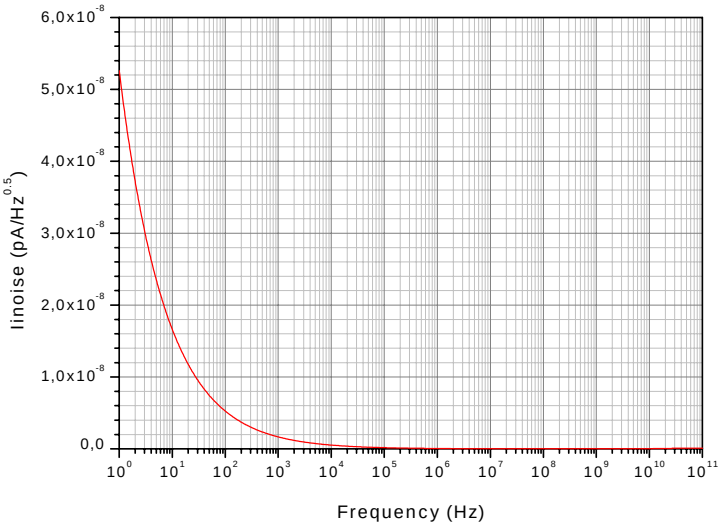


Fig. 11. Input noise current of the transimpedance

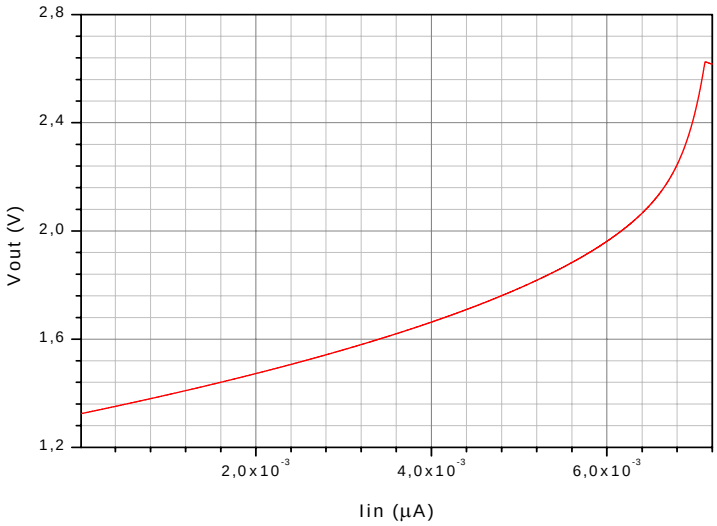


Fig. 12. Output voltage swing as a function of the input photo current

A layout of the proposed TIA (Fig. 13.) has been drawn using 0.35 µm CMOS technology (Nwell, one-poly and two metal layers).

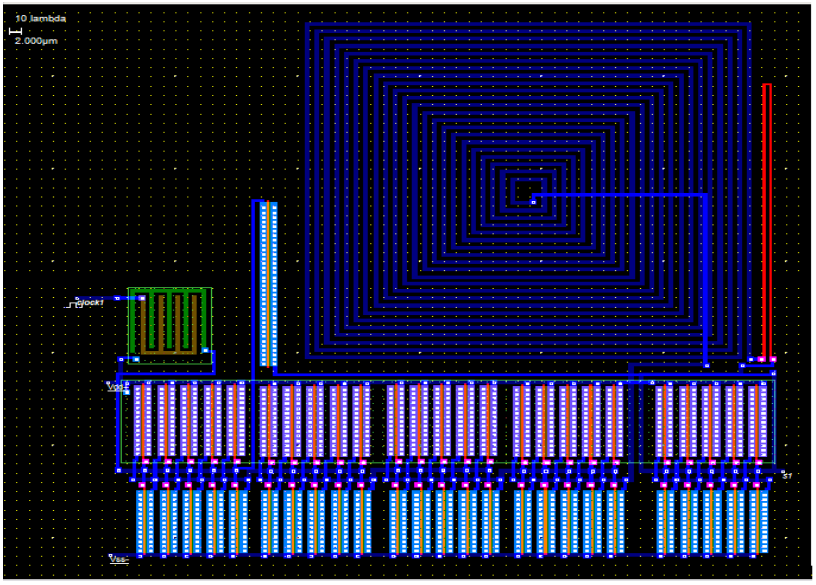


Fig. 13. Layout of the optimized TIA structure

VI. CONCLUSION

High speed integrated optical communication systems will become increasingly ubiquitous given the continual increases in data volume and necessarily higher data transfer speeds.

This paper has presented the preamplifier stage of the optical receiver in a high speed optical communication system. A transimpedance amplifier consisting of a self-biasing inverter string with feedback resistance was proposed to transform small input currents produced by a photodiode to usable voltage levels. It was designed in a low-cost digital 0.35µm CMOS process and is suitable for low voltage Gigabit Ethernet applications. The proposed structure consists of a voltage amplifier with active MOS resistors implementing a local and a global shunt feedback loop. The proposed topology stands out because of its optimal trade-off between power consumption, transimpedance gain and bit rate.

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