INTERPOLATION OF MICROCONTROLLER ADC BY SELF-INDUCED DITHERING

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Abstract- The resolution of ADCs (Analog-to-Digital Converters) can be improved by dithering, i.e. by intentionally injecting white noise into the analog signal. This work describes the theory behind dithering, how to optimize the magnitude of the noise and also a design that illustrates how dithering can be implemented to increase the resolution of a microcontroller's ADC. In order to demonstrate the potential of the design, the resolution of the 10-bit ADC of a PIC18F458 microcontroller is increased to 12 bits by dithering. This is possible by oversampling and decimation. The great advantage of the proposed design is that the noise is generated by the microcontroller itself, obviating the need of an external noise source.

Index terms*: ADC, dithering, resolution, microcontroller, quantization, noise.

I. INTRODUCTION

An analog-to-digital converter (ADC) converts analog voltage samples into integers. An n-bit ADC with a reference voltage U_{ref} has a voltage resolution of

$$\Delta = \frac{U_{ref}}{2^n} \qquad (Eq.1)$$

and it is a general misconception that this sets a limit to the smallest signal changes that can be detected. The inherently limited resolution of any ADC produces a quantization error q that will limit the SNR even in absolutely noise-free analog samples. The maximum quantization error is $\pm \Delta/2$.

There are basically three different ways to increase the ADC's resolution beyond the inherent $\pm \Delta/2$ limit. If the signal bandwidth is limited, simply oversampling the signal will reduce the in-band quantization noise and thereby increase the effective number of bits; each increase of the oversampling rate (OSR) by a factor of four (two octaves) corresponds to a resolution enhancement of one bit [1]. Another common method is to use a noise-shaping ADC-architecture, like a sigma-delta ($\Sigma\Delta$) ADC. A $\Sigma\Delta$ ADC has the inherent property of low-pass filtering the signal and high-pass filtering the quantization noise. Since the quantization noise is pushed towards higher frequencies, the in-band noise is reduced and the effective number of bits increases beyond the theoretical limit [2]. Of course, in order to actually achieve the extra bits of resolution, a number of samples must be averaged (low-pass filtering and decimation) and hence the increase in resolution has a price in terms of reduced data throughput.

The oversampling and noise-shaping ADC techniques are well established and well described in literature [2-5]. The third method that can extend the resolution beyond the theoretical limit is called *dithering*. Dithering means that you deliberately inject additional noise to the analog signal before it is sampled and quantized by the ADC. This is particularly useful in low-resolution ADCs such as ADCs embedded in general-purpose microcontrollers.

To illustrate this, assume we have a 10-bit ADC with reference voltage 3.3 volts. According to Eq. 1, the resolution is 3.3/1024 = 3.223 mV. An input analog sample $s = 1.48$ V would be translated into the integer $|1.48/0.003223| = 459$ by the ADC and if the signal is noise-free (or if

the noise is $\ll \Delta$), the number 459 will be produced every time in a multiple sampling experiment [6]. The output signal histogram would look like in figure 1.
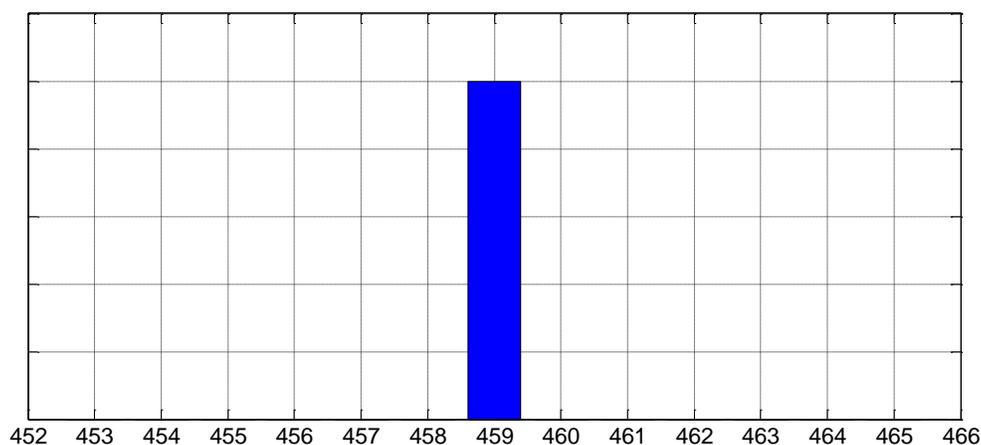

Figure 1. Histogram of low-resolution, un-dithered ADC

However, if we add white Gaussian noise to the signal, with a standard deviation of the same order as Δ, the signal output will be Gaussian with a mean that converges towards the true value *x*, see figure 2.
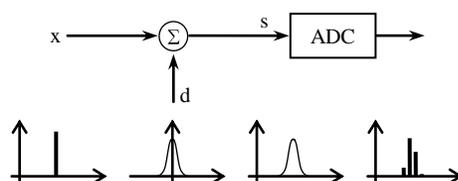

Figure 2. Adding noise changes the pdf

Since the ideal transfer function of the ADC is a staircase function, multiple samples will now be distributed over several integers [7-8], see figure 3. Figure 4 illustrates the histogram of the ADC produced output when the input sample (1.48 volts) has been dithered with white Gaussian noise with an rms equivalent to $\sigma = \Delta$ (a MATLAB simulation). By finding the histogram mean (by averaging) the true sample value can be estimated with a higher resolution than in the un-dithered case.
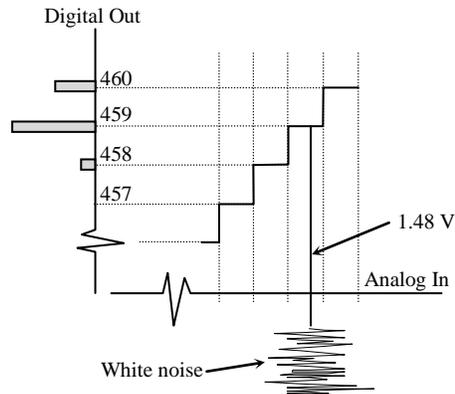
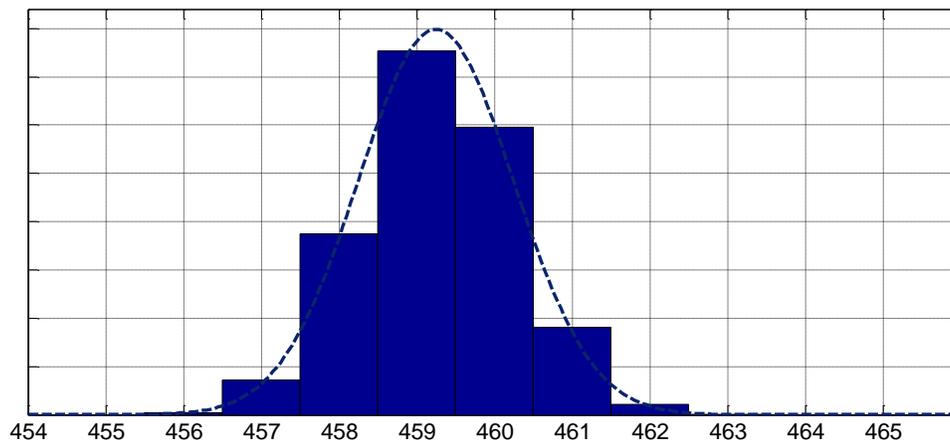Figure 3. Adding noise will distribute the sample over several channels

Figure 4. Histogram of dithered ADC

The theory of dithering is also well described in literature [9-10], but only a few practical implementations for embedded systems have been reported [11-13]. The work presented in this article describes a simple method for implementing dither-based resolution-enhancement in general-purpose microcontrollers with low-resolution ADCs. Some background and related work is presented in section II. Section III presents some theory concerning dithering and section IV presents the hypothesis behind this work. Section V presents the methods and materials used and experimental data are presented and illustrated in section VI and discussed in section VII. In section VIII we summarize this work and draw a few conclusions.

II.   BACKGROUND/RELATED WORK

Dithering as a method for improving the ADC's resolution has been reported by several [6,9-11,14]. However, dithering has also been used to improve the differential linearity in ADCs [15-16] and to increase the frequency resolution in digitally controlled resonant converters [17]. Hewlett-Packard has used large-amplitude dithering in their vector analyzers [7]. Typically, small-amplitude dithering is used to improve ADC resolution, while large-amplitude dithering is used to reduce the ADC non-linearity [8,18].

There are a few different topologies suggested for dither implementations [1,5,15,18], but in principle there are only two basic topologies; subtractive and non-subtractive, see figure 5.
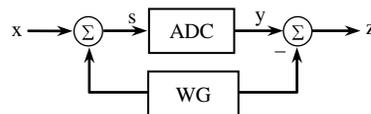
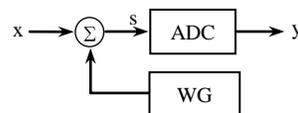

Figure 5a. Subtractive dithering

Figure 5b. Non-subtractive dithering

In this work only the non-subtractive dither topology (with post-filtering) will be considered since this topology provides the best SNR enhancement potential [1].

There is also the question about the spectral distribution of the white noise. There are two obvious choices of white noise; uniformly or Gaussian distributed. The dithering properties of these two different noise distributions have been analyzed by Carbone and Petri [8], Jedrzejewski and Platonov [19] and Petri [18], and it has been established that the achieved dithering effect only weakly depends on the dither signal's distribution [19].

III. THEORY

An n-bit ADC with a reference voltage U_{ref} has a voltage resolution of $\Delta = 1$ LSB as described by Eq. 1 (LSB = Least Significant Bit). The maximum quantization error q introduced by each conversion is $\pm 0.5 \times \Delta = \pm 0.5\,\text{LSB}$. The quantization error q may be anywhere in the interval $\pm 0.5 \times \Delta$, i.e. q is a stochastic variable with a zero mean, uniform distribution. The standard deviation of such a distribution is [20]

$$\sigma_q = \frac{\Delta}{\sqrt{12}} \qquad \text{Eq. 2}$$

For a unipolar ADC with reference voltage U_{ref}, a full-scale sinusoidal would have an amplitude of $U_{ref}/2$ and its rms value would be $U_{ref}/\left(2 \times \sqrt{2}\right)$. Hence, if the quantization noise introduced by the ADC is the only noise present, then we have an (ideal) signal-to-noise ratio (SNR) of

$$\text{SNR}_0 = 20 \times \log\left(\frac{U_{ref}/\left(2 \times \sqrt{2}\right)}{\Delta/\sqrt{12}}\right) = 20 \times \log\left(\frac{2^{n_0} \times \sqrt{12}}{2 \times \sqrt{2}}\right) = 20 \times \log 2^{n_0} + 20 \times \log\sqrt{\frac{12}{8}} =$$

$$= 6.02 \times n_0 + 1.76 \text{ dB} \qquad \text{Eq. 3}$$

Eq. 3 represents the ideal situation; each increment of the ADC's bit resolution will improve the SNR by 6.02 dB. Next we will show how dithering may improve this SNR (and hence the equivalent number of bits of the ADC). First of all, the ADC in figure 2 can be represented by a circuit that adds (quantization) noise to the signal, see figure (6).
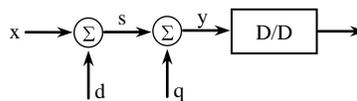

Figure 6. The ADC adds noise to the signal [Carbone and Petri, 1994]

It has been suggested that the dither signal's rms should be of (at least) the same order as the ADC's voltage resolution [7,14]:

$$\sigma_d \approx \Delta \qquad \text{Eq. 4}$$

On the other hand, σ_d should be kept as small as possible in order to increase the acquisition throughput rate [16,21]; the larger the dither noise is, the more samples need to be averaged. If we assume that the quantization noise signal $q(t)$ and the dithering signal $d(t)$ are uncorrelated, then the total noise power in the signal $y(t)$ is $\sigma_q^2 + \sigma_d^2$ and the averaged signal $\overline{y}(t)$ has a noise power of $\left(\sigma_q^2 + \sigma_d^2\right)/N$, where N is the number of samples averaged [21]. Hence, the SNR of a full-scale sinusoidal is

$$\text{SNR} = 20 \times \log\left(\frac{U_{ref}/\left(\sqrt{2}\right)}{\sqrt{\sigma_q^2 + \sigma_d^2}} \times \sqrt{N}\right) = 20 \times \log\left(\frac{U_{ref}/\left(\sqrt{2}\right)}{\sigma_q} \times \frac{\sqrt{N}}{\sqrt{1 + \frac{\sigma_d^2}{\sigma_q^2}}}\right) =$$

$$= 6.02n + 1.76 + 10 \times \log\frac{N}{1 + \frac{\sigma_d^2}{\sigma_q^2}} \qquad\qquad (\text{Eq.}5)$$

Eq. 5 indicates that the SNR will increase if only

$$\frac{N}{1 + \left(\frac{\sigma_d}{\sigma_q}\right)^2} > 1 \quad \Rightarrow \quad N > 1 + \left(\frac{\sigma_d}{\sigma_q}\right)^2 \qquad (\text{Eq.}6)$$

Hence, the larger the dither noise rms is, the more samples will have to be averaged before there is an actual increase in the SNR.

We would also like to know the increase in resolution bits achieved. If we compare Eq. 5 with the SNR of an ideal ADC (Eq. 3), we see that

$$6.02n_0 + 1.76 = 6.02n + 1.76 + 10 \times \log\frac{N}{1 + \left(\frac{\sigma_d}{\sigma_q}\right)^2}$$

$$\Rightarrow \quad 6.02\left(n_0 - n\right) = 10 \times \log\frac{N}{1 + \left(\frac{\sigma_d}{\sigma_q}\right)^2}$$

$$\Rightarrow \quad \Delta n = 1.66 \times \log \frac{N}{1 + \left(\dfrac{\sigma_d}{\sigma_q}\right)^2} \qquad \text{Eq. 7}$$

$$\Rightarrow \quad N = \left(1 + \left(\frac{\sigma_d}{\sigma_q}\right)^2\right) \times 10^{\Delta n/1.66} \qquad \text{Eq. 8}$$

From Eq. 7 we can predict the resolution increase and from Eq. 8 we can predict the number of averages required in order to achieve a certain increase in resolution. For example, if $\sigma_d = 2 \times \sigma_q$, then we need to average 20 samples to gain one extra bit resolution and 1285 samples to increase the resolution by four bits. From these equations it is obvious how important it is to generate a dither signal of the right magnitude.

IV. HYPOTHESIS/DESIGN IDEAS

In order to implement dithering in a microcontroller, there are a few practical problems to solve. First of all, we need a summing circuit that adds noise to the signal. In this work a traditional op amp solution was used [22], see figure 7.
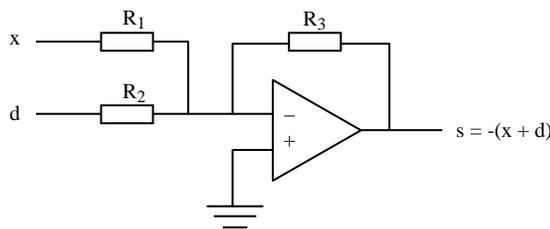

Figure 7. Summing circuit

Secondly, we need a white noise source with a controlled rms level. Typically, electronic noise sources are based on reversed biased p-n junctions in zener diodes or bipolar transistors [23-30], but since our aim here is to improve the performance of a microcontroller, we may take advantage of the intelligence it provides; we use one of its pwm (pulse width modulation) outputs

to generate a (pseudo) random bit sequence. By low-pass filtering this signal, white noise is generated, see figure 8.
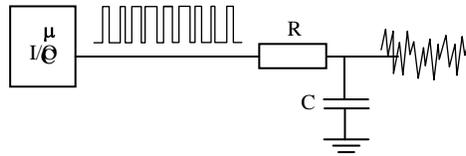

Figure 8. White noise generator

Notice that the low pass filter averages the stochastic pwm signal. That implies that even if the pwm signal has a uniform distribution, the filtered signal will have an (approximately) normal distribution according to the central limit theorem [20]. This solution requires only one single microcontroller I/O-pin and is implementable even in microcontrollers that do not have an embedded pwm unit (most controllers have a pwm unit).

The rms value of the noise generator in figure 8 is of course too large to be immediately used as dither noise, but the rms magnitude is easily reduced to an arbitrary value by resistor R_2 in figure 7.

V. METHODS AND MATERIAL

The proposed design was implemented in a small, 8-bit microcontroller from Microchip, PIC18F458 [31]. As most of Microchips controllers, it has a 10-bit SAR ADC (Successive Approximation Register) and by default it uses the power supply voltage as reference voltage (= +5.00 volts). The design is illustrated in figure 9.

OP1 is used to buffer the input signal. This protects it from being corrupted by the subsequent dithering electronics. OP2 is the summing op amp and OP3 changes the sign of the signal before it is sampled (this is required since the output of OP2 is negative), see figure 7.

The microcontroller was programmed in C. The noise was generated by randomizing the duty cycle of the pwm output. This was achieved by executing *CCPR1L=rand()%256*; in the main C loop (in most C compilers, the *rand()* function produces uniformly distributed unsigned integers).
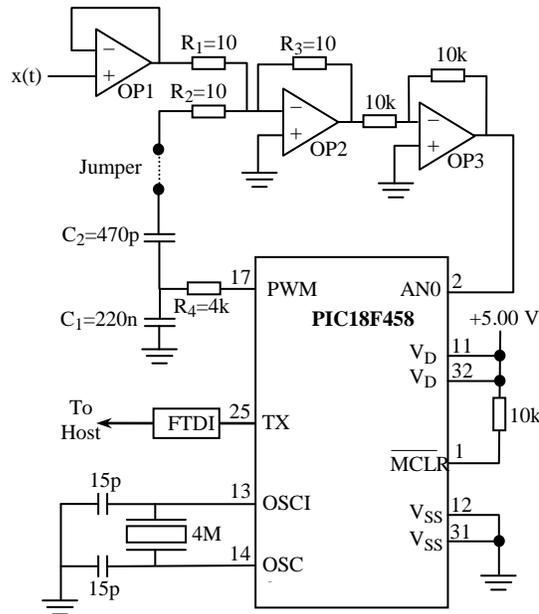
Figure 9. 8-bit microcontroller with dithered ADC

The microcontroller UART was used to transmit data via an asynchronous serial link to a USB port of a host Windows PC. This is possible due to the use of an FTDI chip (Future Technology Devices International) [32], and a Virtual Port Driver (VPD) on the host computer that converts a USB port into a virtual COM port. A terminal program was used to receive the data on the host PC.

R_4C_1 is the low-pass filter that averages the stochastic pwm signal and C_2 removes its DC offset. The jumper makes it possible to conveniently connect/disconnect the dither noise.

In figure 9, $R_1 = R_3$. If the dither signal is $d(t)$ and the analog input signal is $x(t)$, the output of OP2 is

$$-R_3\left(\frac{x(t)}{R_1}+\frac{d(t)}{R_2}\right)=-\left(x(t)+\frac{R_3}{R_2}d(t)\right) \qquad \text{Eq. 9}$$

From Eq. 9 we can see that the rms of the dither signal is easily controlled by resistor R_2. From the theory section III we know that an optimal dither signal should be just large enough to make the quantizer generate only two adjacent integers. If it is too large the data throughput is decreased and if it is too small it may not generate enough noise to produce more than one integer. For a 10-bit ADC with $U_{ref} = 5.00$ volts, $\Delta = 4.88$ mV. The "optimal" dither noise

samples should then be in this range. We will therefore aim for white noise with a 95% confidence interval ($\pm 2\sigma$) of 4.88 mV, i.e. $\sigma = 1.22$ mV; that would generate just enough noise to generate just two integer (in 95% of all cases).

R_1 and R_3 are both 10k resistors (nominal) and R_2 was adjusted until the proper noise was achieved. The noise distribution was measured by setting $x(t)$ to a fixed (low) value (≈ 0) and monitoring the output of OP3 on a digital oscilloscope (TDS5032B). Data was stored and plotted in MATLAB. For $R_2 = 10$ MΩ, we got the noise distribution in figure 10.
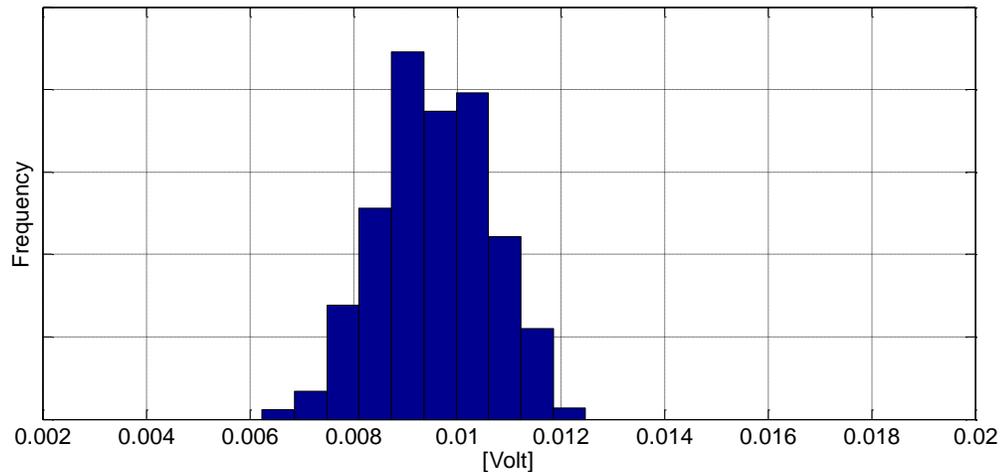

Figure 10. Distribution of dither noise for $R_2 = 10$ MΩ

The noise in figure 9 has a standard deviation of 1.1 mV which means that the 95% confidence interval is 4.44 mV ($\pm 2\sigma$) which is very close to optimal for an ADC with a resolution of $\Delta = 4.88$ mV.

Hence, we have $\sigma_d = 1.11$ mV and $\sigma_q = 4.88 / \sqrt{12} = 1.41\,\text{mV}$. Our aim here is to improve the ADC resolution from 10 to 12 bits and Eq. 8 tells us how many samples we (at least) needs to average:

$$N \geq \left(1 + \left(\frac{1.11}{1.41} \right)^2 \right) \times 10^{2/1.66} = 26$$

VI. EXPERIMENTAL RESULTS

The top diagram in figure 11 illustrates the ADC (10-bit) output for a constant input signal (= +1.747 volts) and no dithering; all samples end up in the same bin (358).

Next, the dither signal was added and 64 samples were added and then down sampled by a factor of 16 which produces the 12-bit number we are aiming for. The lower diagram illustrates a histogram over the ADC output for the same input signal but dithered with the noise in figure 10. Similar data were recorded for other input signal values.
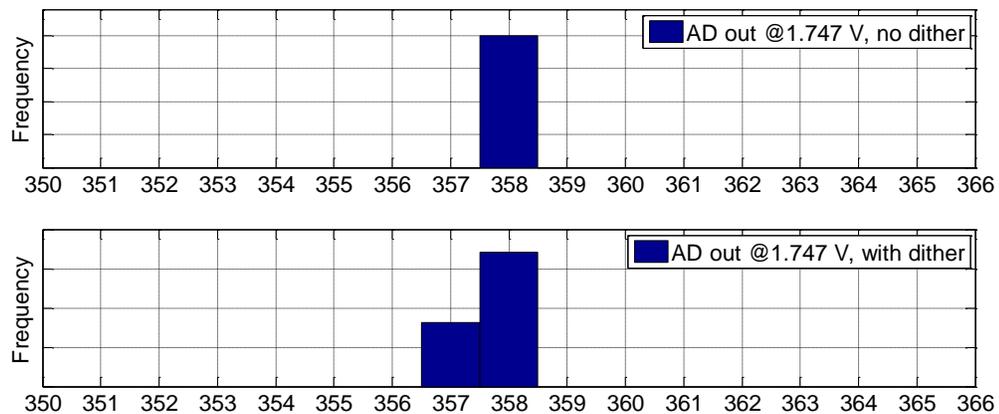

FigURE 11. ADC out distribution with and without dithering

To verify that we indeed have designed a 12-bit ADC, the input-output characteristic was measured over the entire input range of 0 to +5 volts. The result is presented in figure 12.
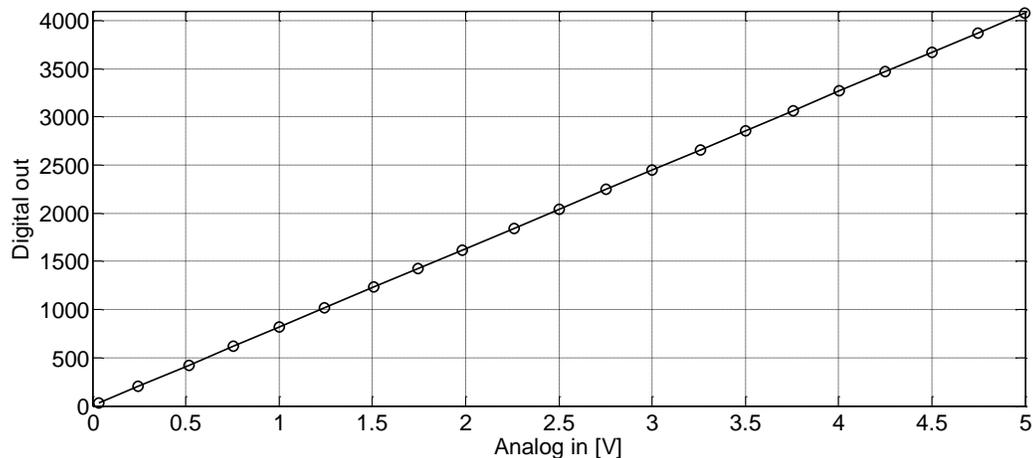
Figure 12. Input-output characteristics of 12-bit ADC

VII. DISCUSSION

Figure 11 clearly illustrates the dithering idea and the potential of the proposed design. The optimal dither noise magnitude "shakes" the input signal just enough to produce two adjacent integers from the 10-bit ADC. This makes it possible to produce a more accurate estimator in software, i.e. increasing the effective number of bits with an optimal data throughput. Figure 12 demonstrates the excellent linearity of the 12-bit ADC; the linearity error was 0.4%.

In the design example presented here, the sampling rate of the 10-bit ADC was 520 S/s. The averaging and down sampling reduced the sampling rate of the 12-bit ADC to just below 10 S/s. There are several ways to improve this sample rate if necessary. First of all, notice that we averaged 64 samples while theory predicted that we need only 26 samples to get the resolution we are looking for; 32 samples with a down sampling factor of 8 would have been sufficient. Secondly, we run the PIC18 with a 4 MHz crystal, but according to the data sheet, we could run it on 40 MHz.

The maximum sampling rate of the 10-bit ADC is determined by the execution time of the loop that takes 64 samples. However, this loops includes the line *CCPR1L=rand()%256*; that generates the noise and it was observed that the execution time of this line was not fixed; the time it takes to execute *rand()%256* depends on the number generated by *rand()*. If that execution time varies, then the sampling rate will vary if a new sampling is initiated manually in the loop. In order to get a fixed sampling rate, the sampling must be triggered by a periodic timer interrupt.

VIII. CONCLUSIONS

Almost all embedded measurement systems depends heavily on the performance of an integrated ADC [33-35] and in order to reduce cost and power consumption, a small microcontroller is typically preferred. Typical microcontrollers only have 8- or 10-bit ADCs. For example, Microchip has no 32-bit microcontroller with more than 10-bits ADC resolution. In embedded measurement systems where microcontrollers are used, this could indeed be a problem. You could solve this problem by adding an external, high-resolution ADC to your design, but that is

costly and requires an interface to the microcontroller, i.e. more hardware/firmware overhead. This work suggests an alternative and it has been demonstrated how proper dithering noise can be generated by the controller itself and how it can be reduced to an optimal magnitude for dithering of a given ADC. The method has been demonstrated by increasing the resolution of an ADC in an 8-bit microcontroller from 10 to 12 bits.

The noise was generated by randomizing the duty cycle of a pwm signal. This method was chosen because it was conveniently available. It could be argued that if you look at the frequency spectrum of the noise, the pwm signal's period will generate a peak in the spectrum (it did indeed), but that does not matter in this particular application; for the method to work, the noise does not have to be perfectly white [19].

Eq. 7 illustrates the delicacy of using dithering; if the noise is too large (or N is too small) the SNR will actually decrease. This work has stressed the importance of generating dither noise of the right magnitude and how to implement it in hardware/firmware.

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