A SENSITIVE DIGITAL MOISTURE DETECTOR FOR NANOSTRUCTURED THIN FILM SENSOR

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Abstract- A digital moisture measuring instrument based on phase angle measuring technique with porous silicon (PSi) or porous alumina (PA) as capacitive moisture sensor is proposed. The proposed technique can measure digitally the phase angle change of capacitive impedance of porous silicon or porous alumina sensor due to change in moisture concentration in terms of clock pulses. Analysis shows that the proposed circuit leads to higher precision by minimizing the errors caused by parasitic earth capacitance as well as offset voltage in the circuit. Simulation and experimental results are reported to confirm the effectiveness of the technique.

Index terms*:* Porous sensors, moisture sensing, digital phase angle measurement, detection circuit.

I. INTRODUCTION

Porous silicon (PSi) and porous alumina (PA) sensors are excellent sensing materials for gas and vapour sensing applications [1-4]. These materials have very high surface to volume ratio 200 - 400 m^2/gm and their morphology can be engineered easily for high selectivity to a particular molecule [2-3]. These features inspire researchers to investigate porous materials for gas and vapour sensing applications. Vapours or gases penetrating into the pores can affect several physical properties of PSi/PA, such as conductivity, dielectric constant and photoluminescence etc. [1,5]. In capacitive PSi/PA sensors due to condensation of vapour molecules in the porous network, the effective dielectric constant of the porous layer increases whereas the conductivity decreases, leading to a change in capacitive impedance of the porous layer which can be represented by RC network [1,4]. In capacitive type moisture sensor based on porous material, the capacitance values are in the range of pF and the change of capacitance values due to change in moisture concentration may be small particularly for ppm level moisture detection [4, 6-8]. Thus to develop a capacitive type sensor care should be taken to measure such small capacitances which play important role for determining the sensitivity of the sensor. Also in such type of sensor, the effect of the parasitic capacitance should be eliminated [8-10]. The present work investigates a simple and suitable measuring circuit, which can measure the phase angle change due to moisture absorption digitally for PSi/PA moisture sensor and minimizes the effect of parasitic capacitance. The circuit is based on phase detection principle when a sinusoidal signal of suitable frequency is passed through a porous layer exposed to gas moisture. The output phase angle of the signal is shifted due to change in capacitance and resistance, caused by moisture condensation inside the porous network of the sensor. The phase angle measurement technique of the capacitive sensor has distinct advantage over the conventional bridge method of measurement. In conventional bridge technique, the unbalanced voltage gets affected due to drift in excitation voltage amplitude, hence bridge technique requires an accurate fixed reference voltage [7-8]. However, in phase angle measurement, the phase shift does not depend on the magnitude of the excitation voltage, rather it depends on phase angle change due to change in capacitive impedance. In sensor based measurement systems, the distant transmission or noisy working environment of analog signal severely degrades the measurement accuracy while sensor data is easily maintained if the sensor output is in digital form. In the applications involving

slowly varying measurands, the conversion of the sensor outputs into signals modulated on the time scale, such as frequency, pulse width, duty cycle offer known advantages in noise immunity, interfacing to digital readout system and achievable resolution [11-12]. The present work proposes a digital capacitive impedance measuring technique for a porous thin film moisture sensing applications. The output is the number of digital clock pulses proportional to phase angle difference caused by the change in moisture concentration of the ambient.

II. DIGITAL PHASE ANGLE MEASUREMENT OF PSi/PA MOISTURE SENSOR

Figure 1 shows the digital phase angle measuring electronics excited by a suitable sinusoidal input voltage signal of relatively low frequency ($V_m \sin wt$). Low measurement frequency is used to improve the sensitivity and to minimize the role of parasitic components of capacitance arising due to different junction formations on the PSi layer [13].

$Z_x (= R_x \parallel C_x)$ is the three terminal capacitive impedance of the actual sensor inside a grounded conducting shield placed at the input of inverting opamp configuration. R_f and C_f are the fixed reference resistance and capacitance at the feedback path of the inverter respectively. The output V_{01} of the first stage inverter is given as

$$V_{01} = -V_s Z_f Y_x, \text{ and admittance } Y_x = \frac{1}{Z_x} = G_x + jwC_x \quad (1)$$

where $G_x (= \frac{1}{R_x})$ is the conductance of the sensor, C_x is the capacitance of the sensor and w is the signal frequency ($2\pi f$) and the impedance $Z_f = \frac{R_f}{1 + jwC_f R_f}$. The output of the first stage inverting configuration is applied to another second stage inverter of gain K. Thus the output of second stage inverter (V_0)

$$V_0 = V_s Z_f Y_x K \quad (2)$$

In polar form, the equation (2) can be written as

$$V_0 = V_m \mid Z_f \mid K \mid Y_x \mid \angle(wt + \phi_1 - \phi_2) \quad (3)$$

where $|Y_x| = \sqrt{G_x^{\,2} + w^2 C_x^{\,2}}$, $\phi_1 = \tan^{-1} wC_x R_x$, $|Z_f| = \dfrac{R_f}{\sqrt{1 + w^2 C_f^{\,2} R_f^{\,2}}}$, $\phi_2 = \tan^{-1} wC_f R_f$, V_m is the peak amplitude of the source voltage. The output of the second inverter and input signals are applied to the comparators to get square wave signals 'a' and 'b' in figure 2. The outputs of comparators are applied to XOR gate, the output of which is pulse width modulated wave 'c'. The output of XOR gate is digitally ANDED with high frequency clock pulses. The output of the AND gate, the wave 'd' is then applied to a counter to obtain the digital word that represents the phase angle ϕ $(= \phi_1 - \phi_2)$ [14]. Figure 2 shows the waveforms timing diagram that illustrates the evaluation of ϕ.

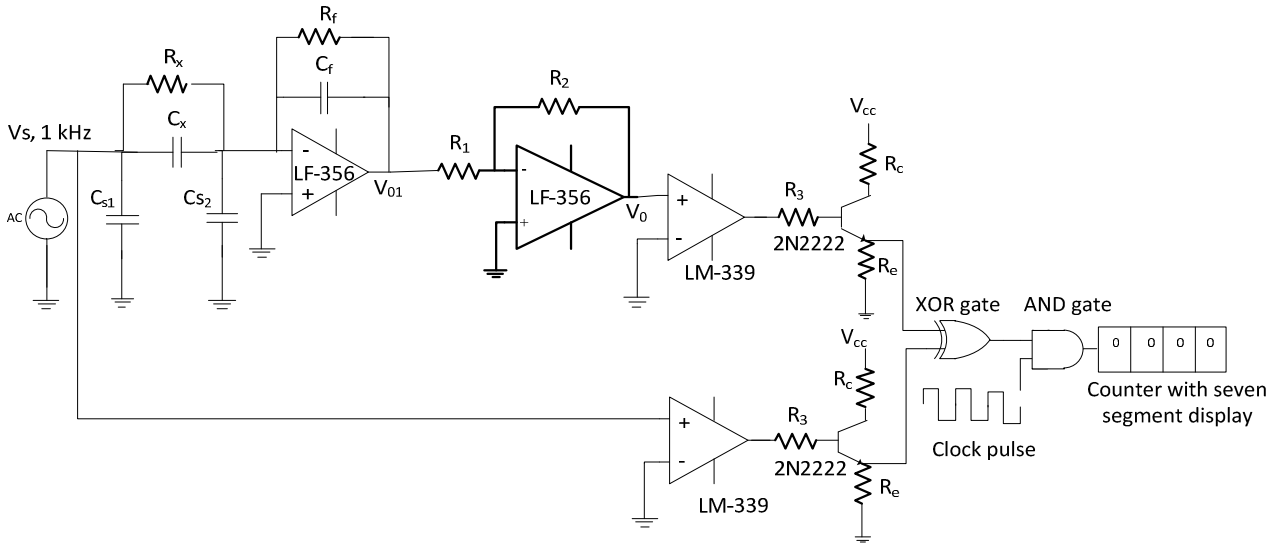


Figure 1. The Digital Phase angle measuring circuit

III. SOURCES OF ERRORS AND THEIR COMPENSATION

a. Effect of parasitic earth capacitance

To achieve high measurement sensitivity and good signal to noise ratio, the effects of stray capacitances on the capacitive impedance measurement should be minimized. A practical capacitance sensor should always have an earthed screen to shield the PSi /PA electrodes from external electrical fields as shown in figure 3(a) [7, 10, 15]. A capacitive sensor enclosed in a earthed conducting shield results in a three terminal sensor consisting of PSi/PA capacitance C_x and the stray capacitances between the electrodes including the leads to the measuring circuit and

the shielding screen C_{s1} and C_{s2}. The values of C_{s1} and C_{s2} are usually from few tens to several hundreds of pF. The equivalent circuit of a practical sensor inside a grounded conducting shield is shown in figure 3(b). Putting the PSi/PA sensor in a conducting shield and grounding the shield one can make the stray capacitances definite. Therefore, if the effects of these capacitances are not eliminated the high sensitivity and the accuracy required of the measuring system will not be obtained. As shown in figure 1, the terminal B of the inverting opamp is at virtual ground potential, thus the stray capacitance C_{s2} is neglected. Similarly, if the impedance of the input voltage source is low and this voltage source is in parallel with the stray capacitance C_{s1}, its effect on the output will be minimum. Thus this simple configuration can minimize the effect of stray capacitances on the measurement of PSi/PA capacitive impedance.

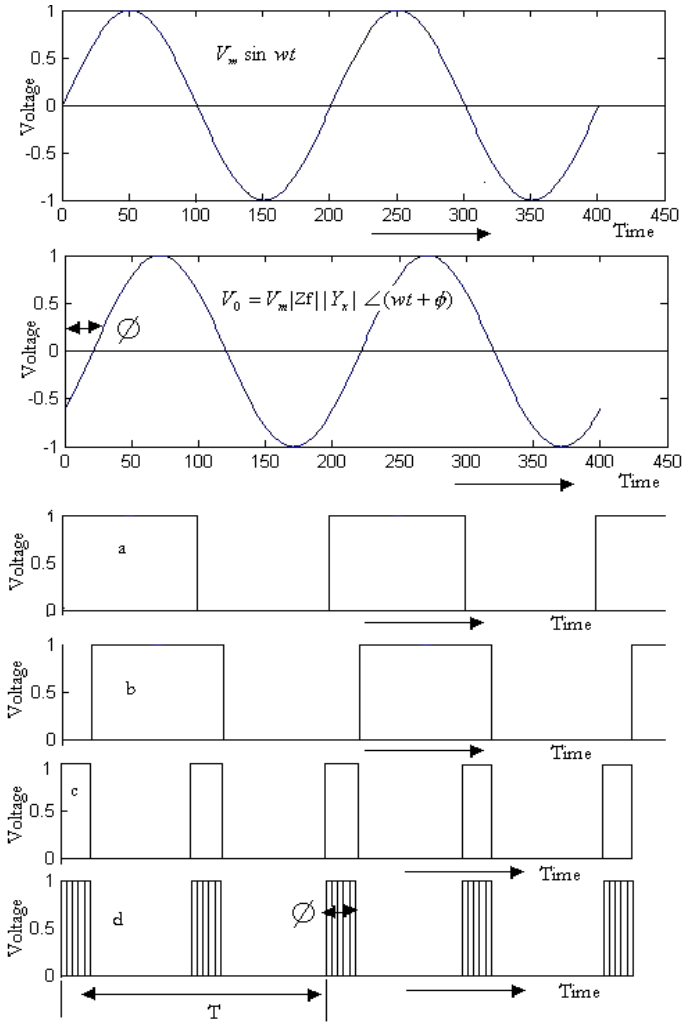
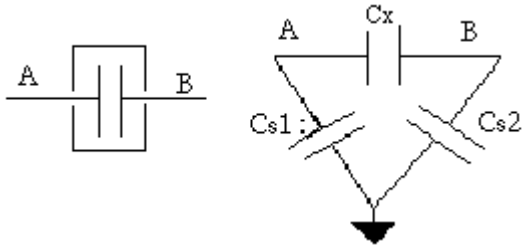


Figure. 2 Waveforms and timing diagram at different stages



(a) (b)

Figure. 3 (a) Three terminal of capacitance, (b) Equivalent form of capacitance

b. Effect of offset voltage

Another source of error is the offset voltage error in the comparator output. Due to offset error of comparators output, XOR gate output will not truly represent the phase angle; thus counter output will be erroneous. However, if the XOR gate inputs (comparator outputs) are processed carefully effect of offset can be minimized. Figure 4 (a) shows timing diagram of the XOR gate and comparator output, when a positive offset for both reference signal and the sensor phase shifted assume equal values are considered. As shown in figure 4 (a), the pulse width of the XOR gate output for both cases with and without offset remains unchanged though the offset affects the comparators output. Figure 4 (b) shows the waveforms when positive offset is considered for sensor's comparator output and the reference signal does not have any offset. A positive offset of sensor output will decrease the pulse width of the first half cycle (say T_1) while it will increase the pulse width of second half cycle (say T_2). In figure 4(b) T_1' and T_2' are the respective ON times of the XOR gate output with positive offset on V_0 . The average of T_1' and T_2' is equal to the average of T_1 and T_2 which are actual ON time when offset in the sensor output is absent [16]. Thus, if the counter is activated for first two consecutive XOR gate output pulses and total counter output is averaged, the results of averaged counter represent true phase angle in terms of clock pulse.

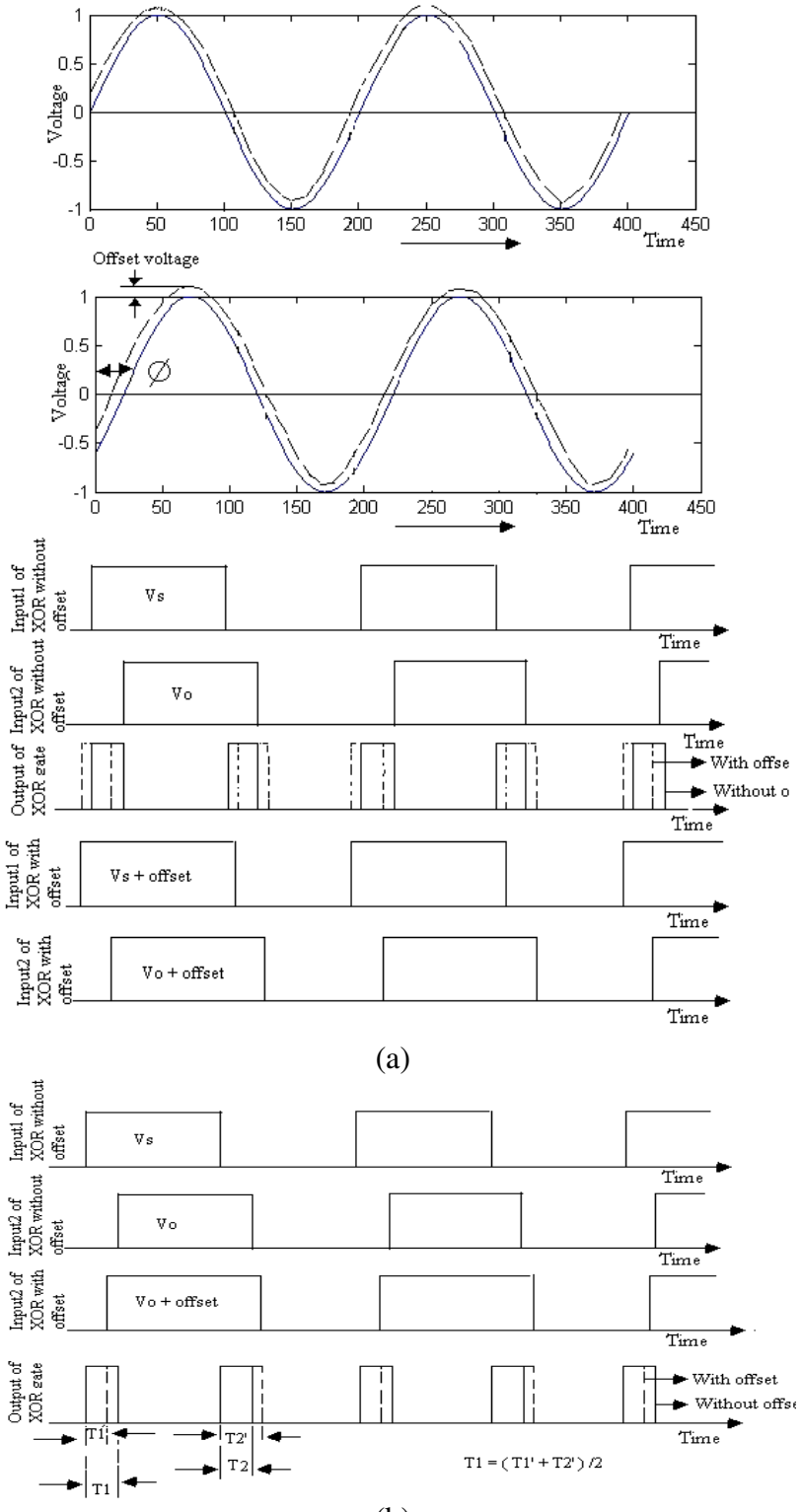


Figure. 4 Waveforms timing diagram for offset compensation (a) when offsets for both comparators output (b) when offset for sensor comparator output

c. Error due to rising and fall times of XOR gate output pulse

Since the XOR gate output decides opening and closing of AND gate there should also be error due to definite rise time of leading edge and fall time of trailing edge of the XOR gate output. If any clock pulse comes within these times counter output will not be able to include these pulses. Figure 5 shows the timing diagram of the waveforms. Here δT is the rise and fall time of XOR gate output. Clock pulses 'a' and 'b' are within the rise and fall times respectively. Thus these pulses will not be included in the counter output. To minimize this error, the clock pulses signal should be selected suitably. The pulses duration of XOR gate output will be much larger than clock pulse duration.

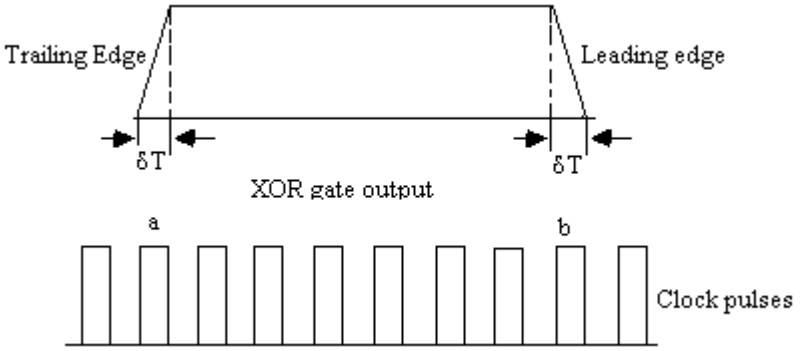


Figure. 5 Effect of rise and fall time for XOR gate output

IV. SIMULATION AND HARDWARE REALIZATION OF THE PROPOSED CIRCUIT

To verify the analysis of the technique, the circuit proposed in figure 1 is simulated by NI MultiSIM software. To simulate the circuit, the excitation voltage of sine wave of amplitude 1 V (rms) and frequency 1 kHz is selected. The first stage inverter is realized by using an opamp with high input impedance, low noise and low offset voltage. Since the sensitivity of both the PSi and PA sensors are different, the feedback resistance R_f and capacitance C_f are selected according to the range of resistance and capacitance values of the sensors with moisture. For PA sensor, the feedback resistance is of 500 kΩ and C_f is of 10 pF. For PSi sensor these values are 30 kΩ and 600 pF respectively. The input impedance of the inverter is the equivalent capacitive impedance of the sensors obtained from experiments with precision LCR meter. The second stage inverter scales the output of the first stage inverter by a constant scaling factor of $K(=\frac{R_2}{R_1}$, where R_2 is a variable

resistance of 10 kΩ and R_1 is a fixed resistance of 10 kΩ). The circuit is also hardware implemented on breadboard. For hardware implementation, the voltage signal of frequency approximately 1 kHz has been generated using a multiphase sinusoidal oscillator as shown in figure 6. The generated voltage source has stable frequency, low harmonic distortion, high current drive capacity and low output impedance. The details of the circuit were discussed elsewhere [17]. The amplitude of the signal is adjusted to 1 V (rms) using a variable pot of 50 kΩ. For impedance matching, buffer is used at different stages of the circuit as shown in figure 6. Both first and second stages are realized by opamp OP-07. The input impedance of the first stage is the parallel combination of discrete ceramic capacitor and metal film resistors, each of 1 % tolerance and the feedback is parallel combination of reference capacitance of 100 pF and 1 MΩ resistance. For both simulation and hardware realization, comparator LM339 is used to obtain two square waves 'a' and 'b' respectively. Waves 'a' and 'b' are now passed through a driver circuits to bring both the amplitudes within 0-5 V. Driver circuits are implemented with two NPN transistors (2N2222). The outputs of drivers are now applied to two inputs XOR gate (74LS136) through digital buffer (74LS244) for comparing the phase of two waves 'a' and 'b'. The output of XOR gate along with wave 'a' and high frequency clock pulse are applied to three inputs AND gate such as 74LS11. Schimitt trigger circuit using CD40106B generates a 500 kHz clock frequency signal. Finally counter CD4029 counts the clock pulses and seven segment displaying unit displays the phase angle in terms of number of clock pulses passing through AND gate.

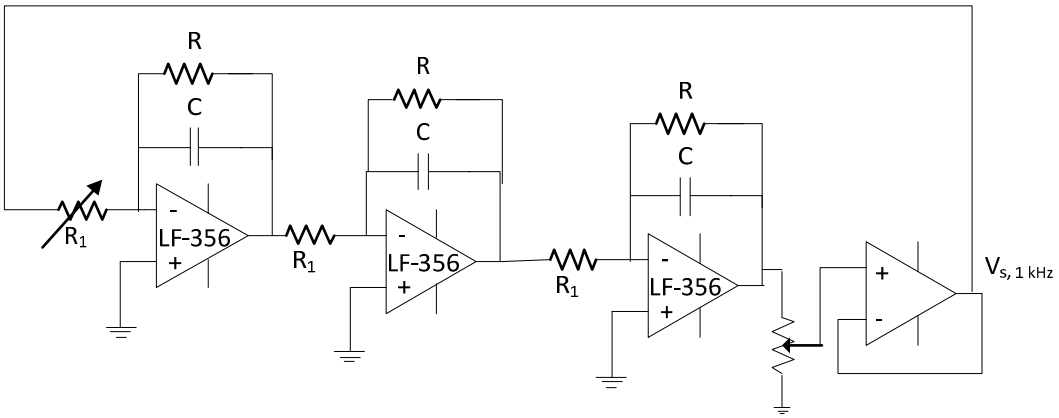


Figure. 6 Inverting mode multi phase sinusoidal oscillator circuit [17]

V. Experimental

a. Sensor testing

The sensors were tested in an in-house designed injection test rig shown in figure 7(a). The photograph of the experimental is reported in [3]. The test chamber was fitted with inlet and outlet gas pipelines. Both PA (ceramic) and PSi sensors are placed inside the chamber, and are connected with a shielded cable of 2 ft long. The reference standard thin film alumina based dew point meter (SHAW, UK) is connected in series path of the pipe line. Thus all the three sensors can be exposed to equal amounts of gas flow having the same concentration of moisture. The chamber was purged with dry blended air at a flow rate of 4 l /m. The sensors for percentage relative humidity sensing has interdigital electrode on the porous film (Psi/PA). The porous silicon sensor has been fabricated by chemical anodization method [4] and the porous alumina film has been fabricated by sol-gel method [2-3]. The thin film of porous alumina is transparent. Figure 7(b) shows the schematic diagram of the sensor structure and figure 7(c) shows the photograph of the sensor.

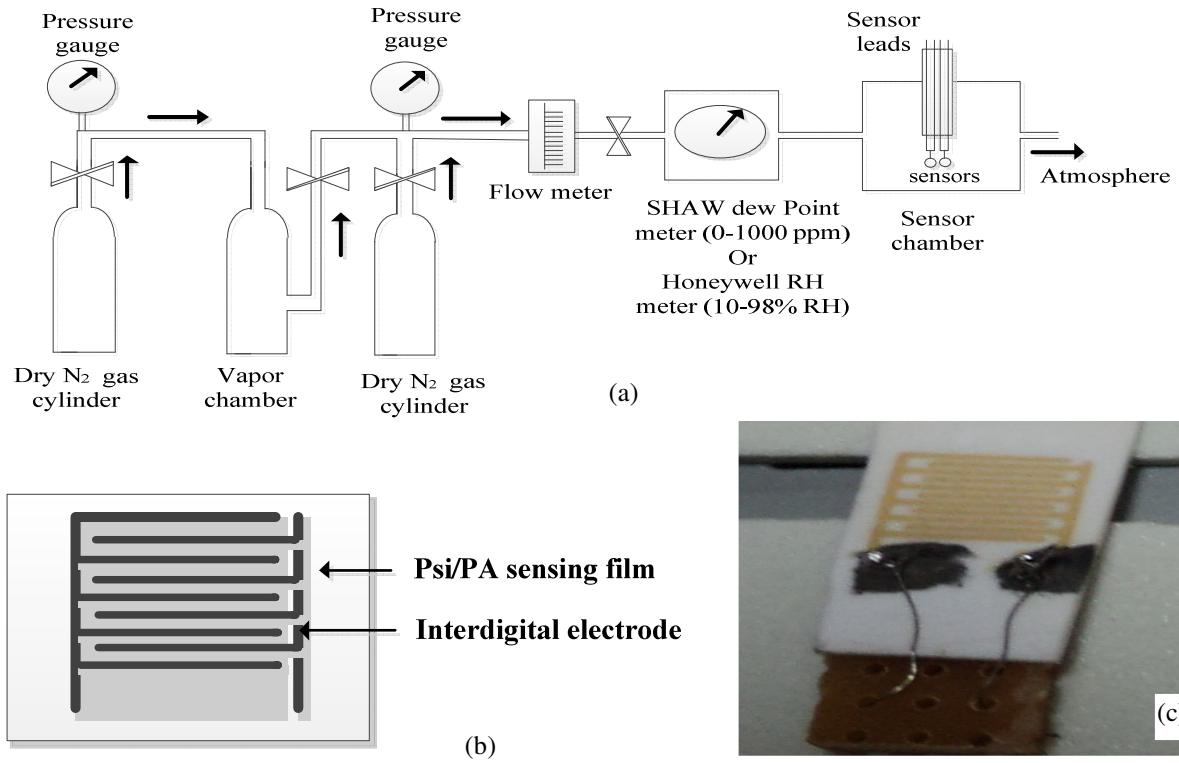


Figure. 7 (a) Schematic diagram of the experimental set-up for humidity detection, (b) schematic of sensor structure (RH level), (c) photograph of PA based RH sensor

The sensors were allowed to equilibrate for several hours prior to testing. Measurements were taken using LCR meter (HP 4284A). The following procedures were adopted:(i) initial base line was adjusted at 6 ppmv of moisture using the standard moisture sensor,(ii) capacitance value of each sensor was noted, (iii) test gas mixture was injected into the chamber and exposed to the sensors**,** (iv) capacitance value of the sensors was measured,(v) concentration of moisture in the gas was increased from 6 ppmv to 200 ppmv and the values of capacitances were measured. The results of the measurements are shown in figure 8 and figure 9. Figure 8 shows the capacitance change with ppm level moisture for porous alumina sensor while figure 9 shows the capacitance change for the porous silicon sensor. The detail experimental procedures as well as sensor fabrication and contact geometry are reported elsewhere [3-5].

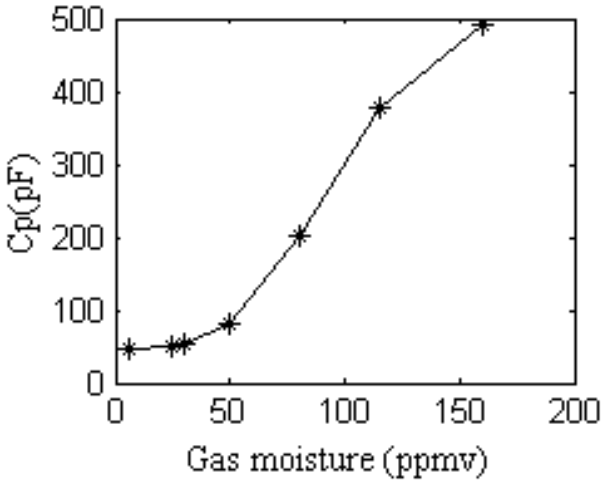


Figure. 8 Experimental plot of capacitance variation with moisture in ppmv of PA sensor (V_s = 1 V rms, f = 1 kHz (HP-4284A))

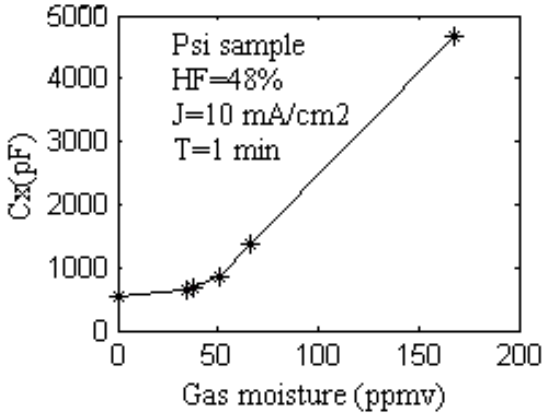


Figure. 9 Experimental plot of capacitance variation with moisture in ppmv of PSi sensor, V_s = 1 V rms, f = 562 Hz (HP-4284A)

b. Results of circuit simulation

The circuit has been simulated with the experimental capacitive impedance values obtained by HP 4284A, LCR meter, which gives C_x, R_x (parallel) values when the actual PSi/PA moisture sensors are exposed to gas moisture of different concentrations. The results of circuit simulation have been represented graphically in figure 10 and 11 respectively. Figure 10 shows counter output in terms of number of clock pulses with moisture level equivalent to the capacitive impedance obtained experimentally for the PA sensor and figure 11 shows the simulation result of the counter output for the PSi sensor. As shown in figure 10, the nature of counter output (clock pulses) variation is almost similar to the capacitance change obtained by LCR meter shown in figure 8. Similarly in figure 11, the nature of clock variation of PSi sensor almost identical to the capacitance variation as ~~of~~ obtained from the LCR meter in figure 9. In order to analyze the effect of parasitic capacitance on the sensitivity of the circuit, two capacitors of 1pF and 10 pF (C_{s1}, C_{s2}) are intentionally connected across the terminals of the sensors. The results of simulation are verified with the results when no parasitic capacitance is considered. It is observed that the effect of parasitic capacitance on the counter output is negligible.

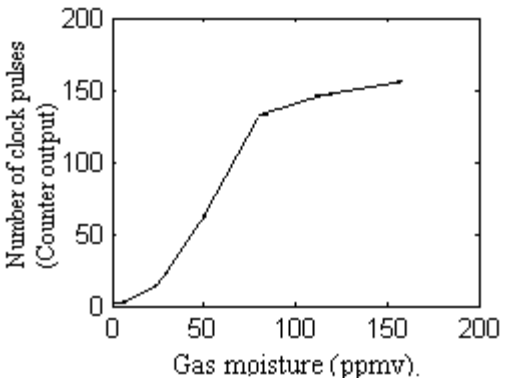


Figure. 10 Simulated plot of counter output for the capacitive impedance with moisture in ppmv of PA sensor, V_s=1 V rms, f = 1 kHz (detection circuit)

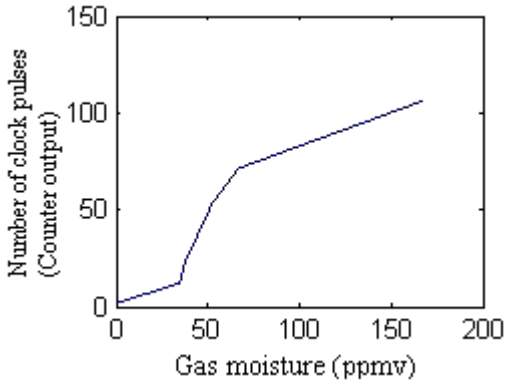


Figure. 11 Simulated plot of counter output for the capacitive impedance with moisture in ppmv of PSi sensor, V_s=1 V rms, f = 562 Hz (detection circuit)

c. Results for hardware implemented circuit

Figure 12 shows the results of hardware-implemented circuit. Here the experiments have been performed with discrete capacitance and resistance values in place of actual sensors. However, the values of capacitance and resistance are of the order of C_x, R_x. The counter output in terms of clock pulse is obviously proportional to change in capacitance and resistance values. Experiments are also performed with the detection circuit for measuring relative humidity (RH) using porous alumina and porous silicon sensor. The experimental set up reported in [3] had been used for the experiments. For PSi, metal contact is coplanar and for porous alumina sandwich metal contact is used. Figure 13 shows the photograph of waveforms taken from CRO (Philips PM 3206) at different points of circuit. XOR gate output, which is pulse duration in tens of microsecond indicates actual phase shift in time scale when the sensors are exposed to moisture.

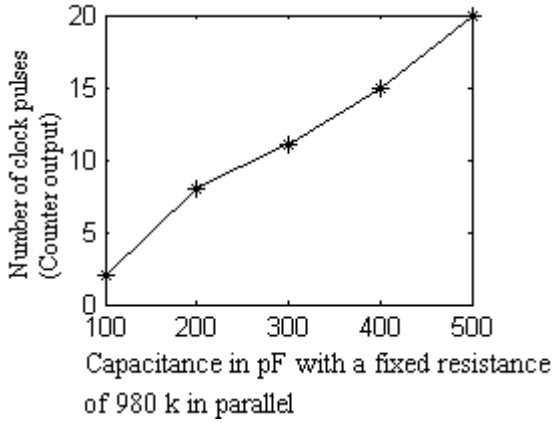


Figure. 12 Plot of output clock pulses with variation of C_x and R_x of the hardware implemented circuit (Vs =1V rms, f = 1 kHz)

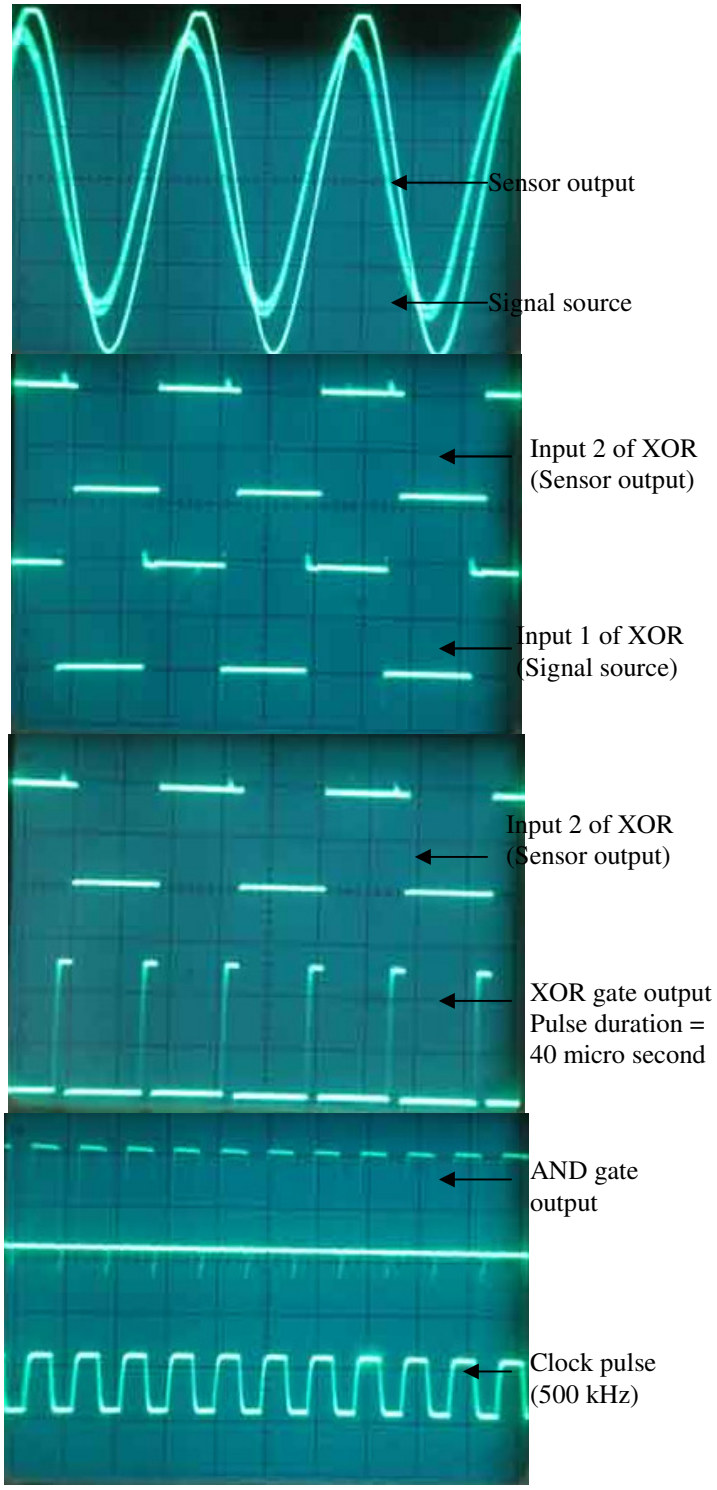
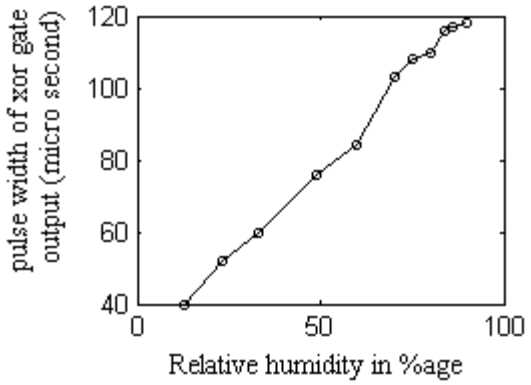
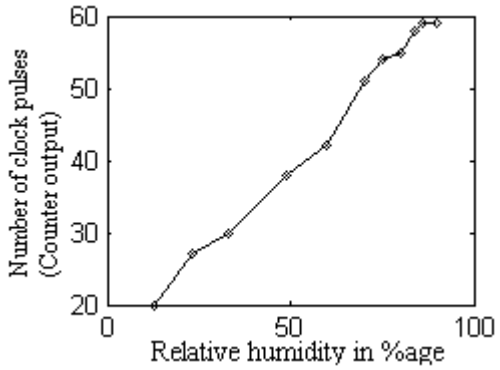


Figure. 13 Photograph of the waveforms taken from CRO (Philips MP 3206) at different points of the circuit

Figure 14 (a) shows the pulse duration of XOR gate output in microsecond for the variation of relative humidity in the vapour chamber with PA sensor and figure 14 (b) is the sensitivity plot, which is the counter output with variation of % relative humidity. Figure 15 shows the sensitivity plot of the PSi sensor with variation of relative humidity. It is evident from the figures that the detection electronics circuit effectively can measure the capacitive impedance change of the sensors.



(a)



(b)

Figure. 14 (a) XOR gate output with variation of relative humidity for porous alumina sensor (Vs = 1V, f = 1kHz) (b) sensitivity plot of porous alumina sensor with proposed circuit (V_s = 1V, f = 1 kHz)

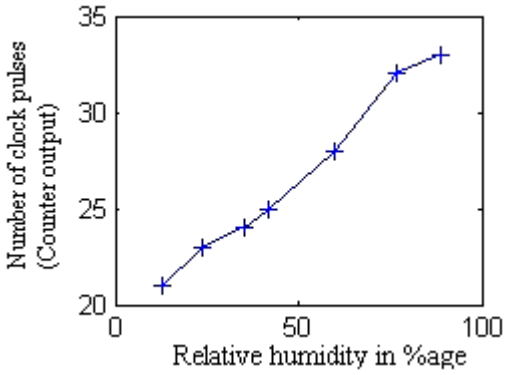


Figure. 15 Sensitivity plot of porous silicon sensor with proposed circuit (PSi formation parameters HF = 48 %, J = 10.5 mA/cm^2, T = 180 sec)

VI. CONCLUSIONS

This paper introduces an accurate digital capacitive impedance measuring technique for porous silicon and porous alumina based moisture sensors. Based on phase detection principle, the technique is simple and provides good resolution and inherently digital readout. It is shown that the non-ideal effects such as, finite open loop gain of opamp and parasitic capacitance, offset voltage of comparators are negligible in the proposed circuit. Its simplicity and compatibility with digital signal processing makes it suitable for read out in a moisture system. Proposed circuit is simple to hardware implement and uses few operational amplifiers and digital devices such as XOR, AND, BUFFER gates, COUNTER etc. Simulations as well as experimental results from hardware realized circuit are shown to verify the theory.

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